1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K60 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

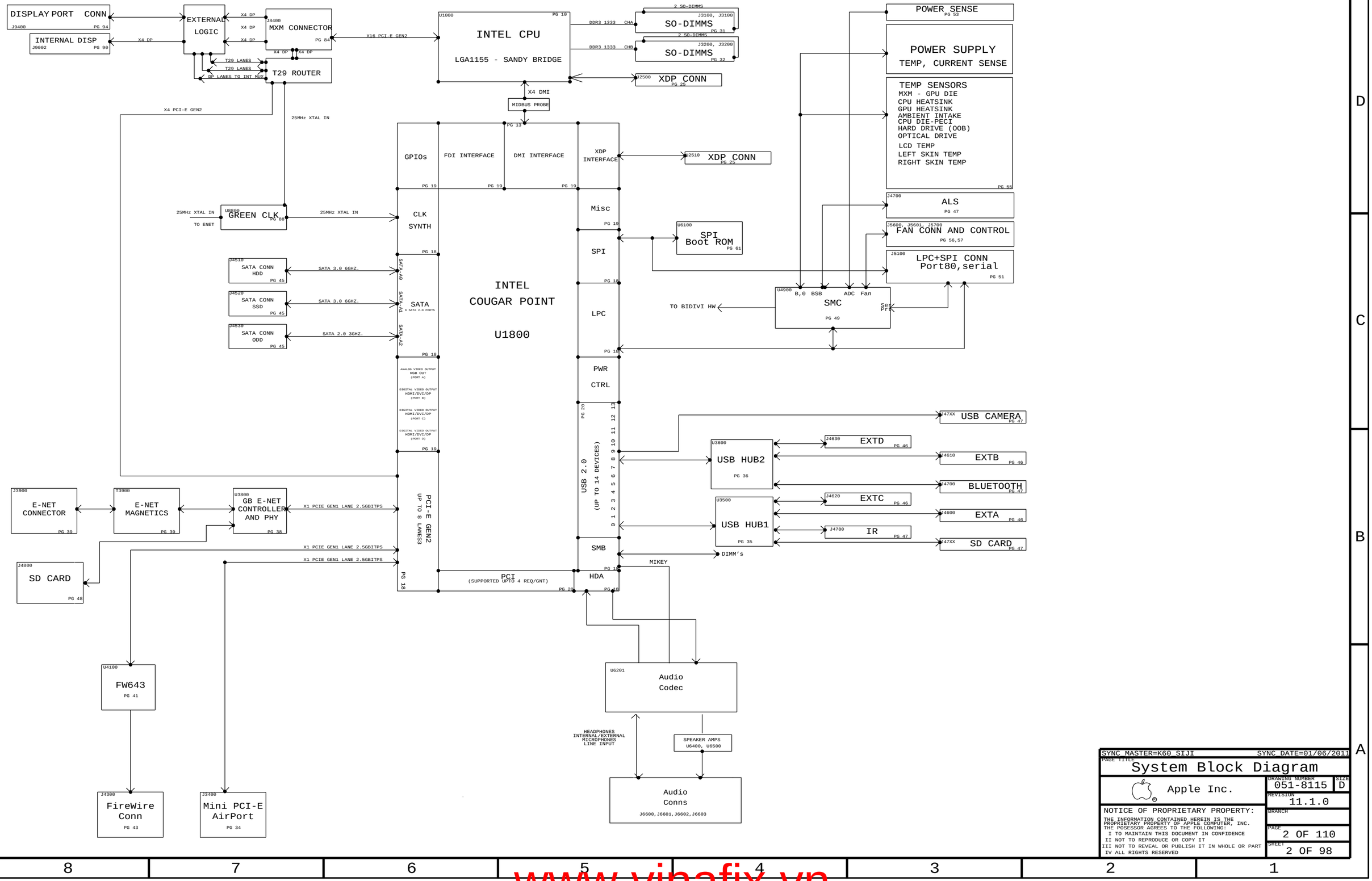
LAST_MODIFIED=Tue Feb 8 14:39:56 2011

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 8 14:39:56 2011

DRAWING TITLE: SCH,K60,MLB

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 98



SYNC_MASTER=K60_SIJI SYNC_DATE=01/06/2011

PAGE TITLE
System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
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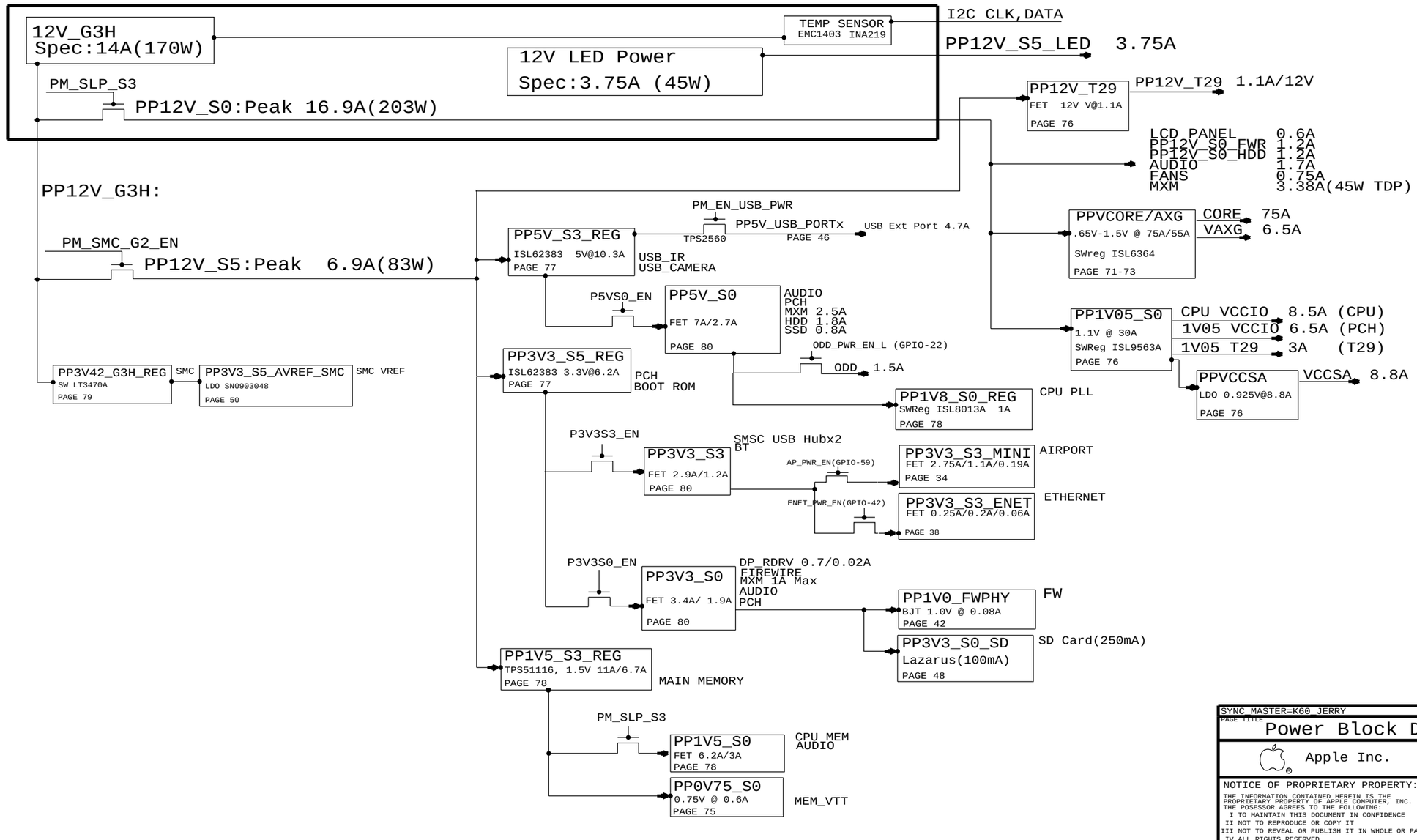
AC/DC POWER SUPPLY (Spec:215W)



SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE: Power Block Diagram

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-0801	PCBA,MLB,DEV,K60	DEVELOPMENT,DEV_GROUP
639-1767	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1820	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1821	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-2160	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2159	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2161	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2118	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2122	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2119	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2132	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2133	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2134	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD
BASIC2	AP,BT,IR,T29
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2452	SUB ASSY,CPU SOCKET,K60,TYCO	TYCO_SOCKET
085-2453	SUB ASSY,CPU SOCKET,K60,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2452	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2453	085-2452		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC,COUGAR POINT,SLJ4F,BD82Z68,PRQ,B3	U1800	CRITICAL	
	353S3055	1	IC,PI3VEDP212,X2 DP MUX,QFN	U9390	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW:	335S0807	1	341T0184	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL
RAW:	335S0539	1	341T0328	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL
	338S0945	1	T29 ROUTER, IC ASSP	U9700	CRITICAL	T29
RAW:	335S0550	1	341T0257	IC,T29,SERIAL EEPROM	U9790	CRITICAL	T29
RAW:	337S3997	1	341T0326	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29
RAW:	335S0709	1	341T0330	IC,MXM SYS ROM,24C02	U8570	CRITICAL	
RAW:	338S0878	1	341T0185	IC,SMC,K60	U4900	CRITICAL	K60

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4043	1	SNB,SR00S,PRQ,D2,2.5,65W,4+1,6M,LGA	CPU	CRITICAL	2P5GHZ_SNB_CPU_PRQ
337S4062	1	SNB,SR009,PRQ,D2,2.7,65W,4+1,6M,LGA	CPU	CRITICAL	2P7GHZ_SNB_CPU_PRQ
337S4061	1	SNB,SR00E,PRQ,D2,2.8,65W,4+1,8M,LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU_PRQ

K60 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8115	1	SCH,MLB,K60	SCH1		K60
820-2641	1	PCBF,MLB,K60	MLB1		K60

K60 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293			330UF
371S0679	371S0652			PIN DIODE
377S0107	377S0066			USB DIODE
376S0972	376S0612			ROHM TRA-BJT

SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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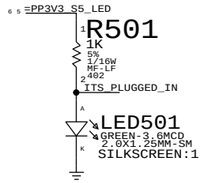
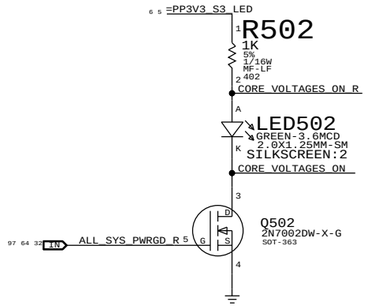
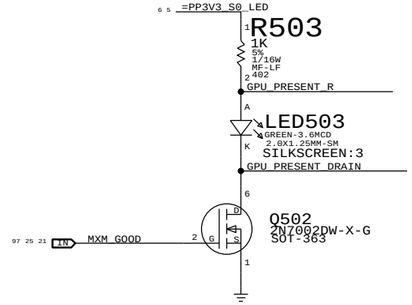
S5 Led



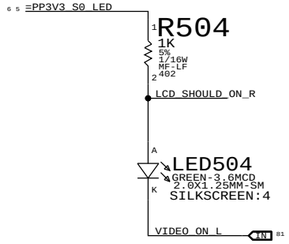
ALL_SYS_PWRGD Led



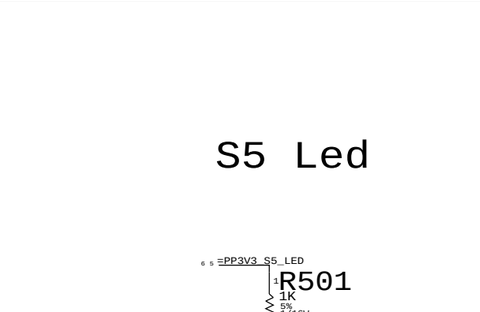
MXM PWR GOOD Led

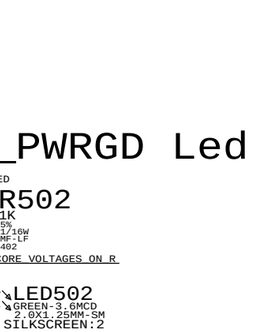


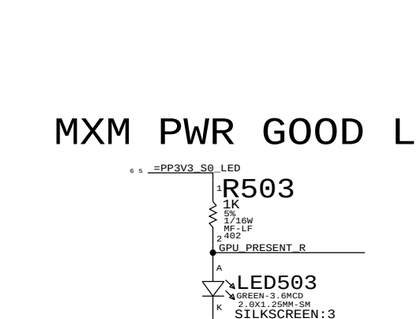
VIDEO ON Led

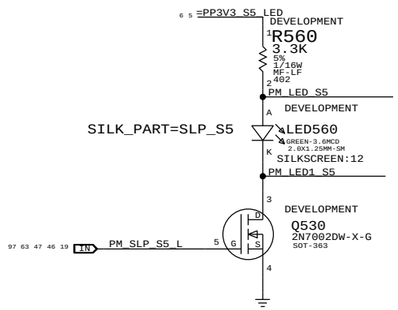


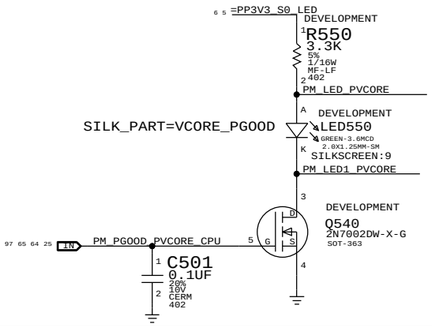
PROTO DEBUG LEDS ARE SHOWN BELOW

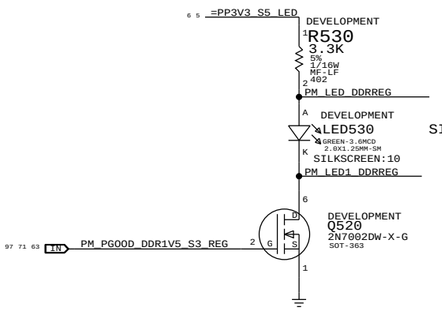


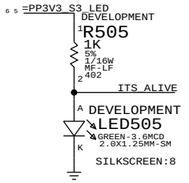












SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER	051-8115
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REVISION	11.1.0
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POWER SUPPLY TO MLB

J600
76833-0106
M-RT-TH

518-0373

PP12V_G3H_ACDC 6
PP12V_S0_PS 6

C611 1UF 10% 25V X5R 603-1
PLACE C611 CLOSE TO CONNECTOR

C610 1UF 10% 25V X5R 603-1
PLACE C610 CLOSE TO CONNECTOR

MLB TO BLC

94 81 49 BI SMB_BLC_TCON_SDA
94 81 49 IN SMB_BLC_TCON_SCL

R630 0 1/16W 402 5%
R631 0 1/16W 402 5%
SMB_BLC_TCON_SDA_R
SMB_BLC_TCON_SCL_R

NOSTUFF C627 47PF 5% 50V CERM 402
NOSTUFF C628 47PF 5% 50V CERM 402

49 6 =PP3V3_S0_SMBUS

FET DIODE IS S TO D (FACES BLC WHICH 3V3 RISES BEFORE MLB 3V3).

NOSTUFF C621 47PF 5% 50V CERM 402
Q600 2N7002DW-X-G SOT-363

49 BI =SMB_BLC_PCH_SDA
49 IN =SMB_BLC_PCH_SCL

NOSTUFF R618 0 1/16W 402 5%
NOSTUFF R617 0 1/16W 402 5%
SMB_BLC_PCH_SDA_R
SMB_BLC_PCH_SCL_R

BLC SDA/SCL ISOLATION CIRCUIT

NOSTUFF C622 47PF 5% 50V CERM 402
Q600 2N7002DW-X-G SOT-363

R622 0 1/16W 402 5%
91 21 15 IN BLC_GPIO
BLC_GPIO_R

L602 FERR-1000-OHM 0402
97 81 IN VSYNC_DP_CONN
VSYNC_DP_CONN_R

CRITICAL
J602
53780-8608
F-RT-SM

518S0543

ISOLATED_GND
R620 0 5% 1/16W MF-LF 402

MLB TO PS

PLACE C606 CLOSE TO CONNECTOR

97 63 IN PM_EN_P12V_S0_FET
Q610 2N7002 SOT23-HF1
C606 0.001UF 10% 50V X7R 402

R602 0 1/16W 402 5%
49 IN =SMB_ACDC_SCL
SMB_ACDC_SCL_RC

R601 0 1/16W 402 5%
49 BI =SMB_ACDC_SDA
SMB_ACDC_SDA_RC

PS_ON
R605 0 1/16W 402 5%
ISOLATED_GND2

97 81 BL_EN
97 83 BL_PWM

C604 47PF 5% 50V CERM 402
C602 47PF 5% 50V CERM 402
C603 0.001UF 10% 50V X7R 402
PLACE C603 CLOSE TO CONNECTOR

CRITICAL
J601
50293-00771-H01
M-ST-SM

518S0813

95 PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_DDR_LDO 71
=PP0V75_S0_MEM_VTT_S0FET 32

95 PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_DDR_FET 32
=PP0V75_S0_MEM_VTT_B 31
=PP0V75_S0_MEM_VTT_A 30

95 PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU_REG 66
=PPVCORE_S0_CPU 13 16 50 65

95 PPVAXG_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVAXG_S0_REG 67
=PPVAXG_S0_CPU 13 17 50 65

95 PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_S0_REG 68
=PP1V05_S0_PWR 50
=PPVCCIO_S0_XDP 25
=PPVCCIO_S0_CPU 10 11 13 16 65
=PPVCCIO_S0_SMC 46 47
=PP1V05_S0_PCH_PWR 50
=PPVCCSA_S0_INPUT_PWR 50 69
=PP1V05_S0_CK505 26

95 PP1V05_S0_PCH
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_S0_PCH_SNS 50
=PP1V05_S0_PCH_VCC_DMI 22 24
=PP1V05_S0_PCH_VCCADPLL 17
=PP1V05_S0_PCH_VCCIO_DMI 22 24
=PP1V05_S0_PCH_VCCIO_SATA 18 22 24
=PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
=PP1V05_S0_PCH_VCC_CORE 22 24
=PP1V05_S0_PCH_VCCIO_USB 22 24
=PP1V05_S0_PCH 18 24 79
=PP1V05_S0_PCH_VCCDIFFCLK 22 24
=PP1V05_S0_PCH_VCCSSC 22 24
=PP1V05_S0_PCH_V_PROC_IO 22 24
=PP1V05_S0_PCH_VCCASW 22 24
=PP1V05_S0_P1V05T29FET 80

95 PP1V05_S0_INPUT_VCCSA
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCCSA_S0_INPUT_SNS 50
=PPVCCIO_S0_CPU_VCCSA 69

95 PPVCCSA_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=0.925V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCCSA_S0_FET 69
=PPVCCSA_S0_CPU 13 50
=PPVCCSA_S0_PWRCTL 64

95 PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_FET 73
=PP1V5_S0_AUD_DIG 56
=PP1V5_S0_CK505 26
=PP1V5_S0_MINI 33
=PP1V5_S0_PWR 50
=PP1V5_S0_DP 83

95 PP1V5_S0_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_MEM_SNS 50
=PP1V5_S0_CPU_MEM 11 13 16 28 29

95 PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FET 73
=PP3V3_S0_PCH 18 21 24
=PP3V3_S0_FAN 53 54
=PP3V3_S0_PCH_VCCADAC 17
=PPSPD_S0_MEM_A 30 47
=PPSPD_S0_MEM_B 31
=PP3V3_S0_AUDIO 56 58 59 60 61 62
=PP3V3R1V5_S0_PCH_VCCSUSHDA 24
=PP3V3_S0_SMBUS 6 49
=PP3V3_S0_SMC_LS 47 51
=PP3V3_S0_SMBUS_SMC_0 49
=PP3V3_S0_SMBUS_SMC_B 49
=PP3V3_S0_SMBUS_SMC_MGMT 49
=PP3V3_S0_MXM 21 64 75 76
=PP3V3_S0_ODD 42
=PP3V3_S0_SATALED 18 42
=PP3V3_S0_SENSE 50 52
=PP3V3_S0_PWRCTL 63 64 73 80
=PP3V3_S0_PCH_VCC3_3_GPIO 22 24
=PP3V3_S0_FWPHY 39 40 41
=PP3V3_S0_DP 81
=PP3V3_S0_PCH_VCC3_3_PCI 22 24
=PP3V3_S0_CK505 26
=PP3V3_S0_PCH_GPIO 20 45
=PP3V3_S0_PCH_STRAPS 15
=PP3V3_S0_PCH_VCC3_3_SATA 22 24
=PP3V3_S0_RSTBUF 11 27
=PP3V3_S0_PCH_PM 27
=PP3V3_S0_SMBUS_SMC_BSA 49
=PP3V3_S0_SDCARD 45
=PP3V3_S0_P1V05_VREG 68
=PP3V3_S0_PCH_VCC3V3 22 24
=PP3V3_S0_VRD 65 68
=PP3V3_S0_LED 5
=PP3V3_S0_P3V3T29FET 80
=PP3V3_S0_DPSDRVA 84
=PP3V3_S0_INTDPMUX 83
=PP3V3_S0_T29PWRCTL 80
=PP3V3_S0_T29I2C 49
=PP3V3_S0_ENET_PHY 36 37

"S0" RAILS

ONLY ON IN RUN

95 PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V8_S0_REG 71
=PP3V3R1V8_S0_PCH_VCCDFTERM 22 24
=PP1V8R1V5_S0_PCH_VCCVRM 24 79
=PP1V8_S0_CPU_PLL 13 16
=PP1V8_S0_PCH 19
=PP1V8_S0_PWRCTL 64

98 95 PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S0_FET 73
=PP5V_S0_AUDIO 56
=PP5V_S0_SATA 42
=PP5V_S0_MXM 75
=PP5V_S0_VRD 65 67
=PP5V_S0_ISENSE 50
=PP5V_S0_PCH 24
=PP5V_S0_P1V05_VREG 68
=PP5V_S0_LPCPLUS 48
=PP5V_S0_P1V8_REG 71

95 PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.5mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S0_PS 6
=PP12V_S0_AUDIO_SPKRAMP 58 59
=PP12V_S0_VRD 65
=PP12V_S0_MXM_PWR 50
=PP12V_S0_LCD 81
=PP12V_S0_P1V05_VREG 68
=PP12V_S0_PWRCTL 63 64 80
=PP12V_S0_SENSE 51
=PP12V_S0_FW 41
=PP12V_S0_CPU_VCCSA 69
=PP12V_S0_SATA 42
=PP12V_S0_FAN 53 54

95 PP12V_S0_MXM
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S0_MXM_SNS 50
=PP12V_S0_MXM 75

"S3" RAILS

ON IN RUN AND SLEEP

95 PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_REG 71
=PP1V5_S3_MEM_PWR 50
=PP1V5_S3_S0FET 73

95 PP1V5_S3_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_SNS 50
=PP1V5_S3_MEMRESET 32
=PP1V5_S3_MEM_A 28 29 30
=PP1V5_S3_MEM_B 28 29 31

98 95 PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_FET 73
=PP3V3_S3_BT 44
=PP3V3_S3_SMBUS_SMC_A 49
=PP3V3_S3_MINI 33
=PP3V3_S3_PWRCTL 64 73 82
=PP3V3_S3_MEMRESET 32
=PP3V3_S3_USB_HUB 34 35
=PP3V3_S3_ENET_PHY 36
=PP3V3_S3_SDCARD 44 45
=PP3V3_S3_VREFMRGN 28
=PP3V3_S3_VRD 71
=PP3V3_S3_LED 5
=PP3V3_SW_DPAPWR 78
=PP3V3_S3_SYSCLK 79
=PP3V3_S3_P3V3R2V9_REG_A 82
=PP3V3_S3_PCH 21

98 95 PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S3_REG 70
=PP5V_S3_USB 43
=PP5V_S3_S0FET 73
=PP5V_S3_CAMERA 44
=PP5V_S3_IR 44
=PP5V_S3_MEMRESET 32
=PP5V_S3_DDR_VREG 71
=PP5V_S3_VREFMRGN 28
=PP5V_S3_P3V3R2V9_REG_A 82

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

95 PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_REG 70
=PP3V3_S5_PCH 18 19 21 24
=PP3V3_S5_PCH_GPIO 20
=PP3V3_S5_ROM 48 55
=PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
=PP3V3_S5_PWRCTL 11 63 64
=PP3V3_S5_S3FET 73
=PP3V3_S5_S0FET 73
=PP3V3_S5_PCH_STRAPS 15
=PP3V3_S5_XDP 25
=PP3V3_S5_LPCPLUS 48
=PP3V3_S5_PCH_VCCDSW 22 24
=PP3V3_S5_USB_HUB 34
=PP3V3_S5_CPU_VCCSA 69
=PP3V3_S5_PCH_VCCSPI 22 24
=PP3V3_S5_VRD 70
=PP3V3_S5_LED 5
=PP3V3_S5_MEMRESET 32
=PP3V3_S5_RSTBUF 27
=PP3V3_S5_P3V3R2V9_A 82
=PP3V3_S5_SMCUSBMUX 43
=PP3V3R1V5_S5_PCH_VCCSUSHDA 24

95 PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S5_LDO 70
=PP5V_S5_PCH 24

95 PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FET 74 95
=PP12V_S5_DDR_VREG 71
=PP12V_S5_P5VS3_VREG 70
=PP12V_S5_PWRCTL 33 64 73
=PP12V_S5_T29_A 82

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

95 PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V42_G3H_REG 72
=PP3V3_G3H_RTC_D 27
=PP3V3_G3H_SMC 46 47
=PP3V3_G3H_SMCUSBMUX 43
=PP3V3_G3H_LPCPLUS 48

95 PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_G3H_ACDC 6
=PP12V_G3H_S5_FET 74
=PP12V_G3H_3V42 72

T29 RAILS

95 PP3V3_S0_T29
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_T29_FET 80
=PP3V3_T29_RTR 79 80 86 87

95 PP1V05_S0_T29
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_T29_FET 80
=PP1V05_T29_RTR 87
=PP1V05_T29 80

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

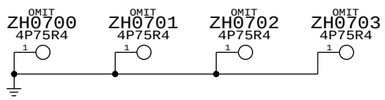
SYNC_MASTER=K60_MARK SYNC_DATE=12/30/2010
PAGE TITLE
Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 6 OF 110
SHEET 6 OF 98

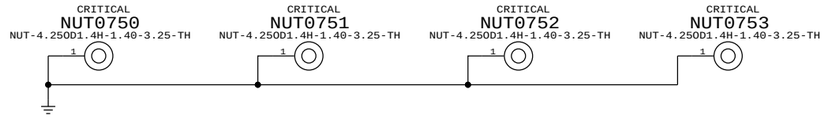
CPU Heatsink

4mm Plated Holes (998-0850)



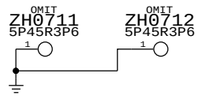
DIMM CONNECTOR NUTS

Nuts (805-9582)



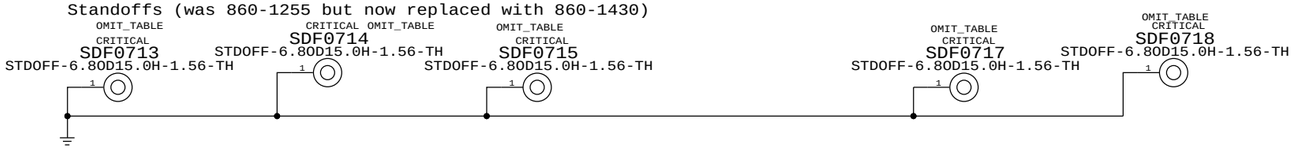
PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)



Rear Cover

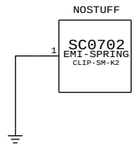
Standoffs (was 860-1255 but now replaced with 860-1430)



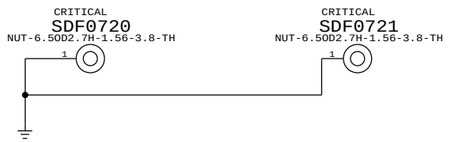
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	5	STANDOFF,MLB,K60/K62	SDF0713,SDF0714,SDF0715,SDF0717,SDF0718	

For EMC

EMC Spring (870-1577); Near DIMMs



MXM STANDOFFS (835-0272)



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 7 OF 110

SHEET: 7 OF 98

UNUSED CPU SIGNALS

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE

18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERN4	NC_PCIE_D2R_PERN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERP4	NC_PCIE_D2R_PERP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETN4	NC_PCIE_R2D_PETN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETP4	NC_PCIE_R2D_PETP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20	TP_USB_1N	NC_USB_1N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_1P	NC_USB_1P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2N	NC_USB_2N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2P	NC_USB_2P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3N	NC_USB_3N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3P	NC_USB_3P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4N	NC_USB_4N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4P	NC_USB_4P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5N	NC_USB_5N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5P	NC_USB_5P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6N	NC_USB_6N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6P	NC_USB_6P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7N	NC_USB_7N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7P	NC_USB_7P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12N	NC_USB_12N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12P	NC_USB_12P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13N	NC_USB_13N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13P	NC_USB_13P	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

10	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

UNUSED SIGNAL ALIAS

Apple Inc.

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PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

18 IN PEG_CLK100M_P — 90 GPU_CLK100M_PCIE_P — CLK_100M_MXM_P OUT 75
MAKE_BASE=TRUE

18 IN PEG_CLK100M_N — 90 GPU_CLK100M_PCIE_N — CLK_100M_MXM_N OUT 75
MAKE_BASE=TRUE

19 IN =PEG_R2D_C_P<0..15> — PEG_R2D_C_P<0..15> OUT 77 90
MAKE_BASE=TRUE

19 IN =PEG_R2D_C_N<0..15> — PEG_R2D_C_N<0..15> OUT 77 90
MAKE_BASE=TRUE

19 OUT =PEG_D2R_P<0..15> — PEG_D2R_P<0..15> IN 77 90
MAKE_BASE=TRUE

18 OUT =PEG_D2R_N<0..15> — PEG_D2R_N<0..15> IN 77 90
MAKE_BASE=TRUE

21 IN PEG_CLKREQ_L — MXM_CLKREQ_L OUT 75 97
MAKE_BASE=TRUE

75 MXM_RESET_L — PEG_RESET_L 27 97
MAKE_BASE=TRUE

97 91 19 IN PM_CLK32K_SUSCLK_R — R929 22 1 2 — PM_CLK32K_SUSCLK OUT 46 91 97
PLACEMENT_NOTE=PLACE CLOSE TO U1800
5% 1/10W MF-LF 402

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: Signal Aliases

Apple Inc.

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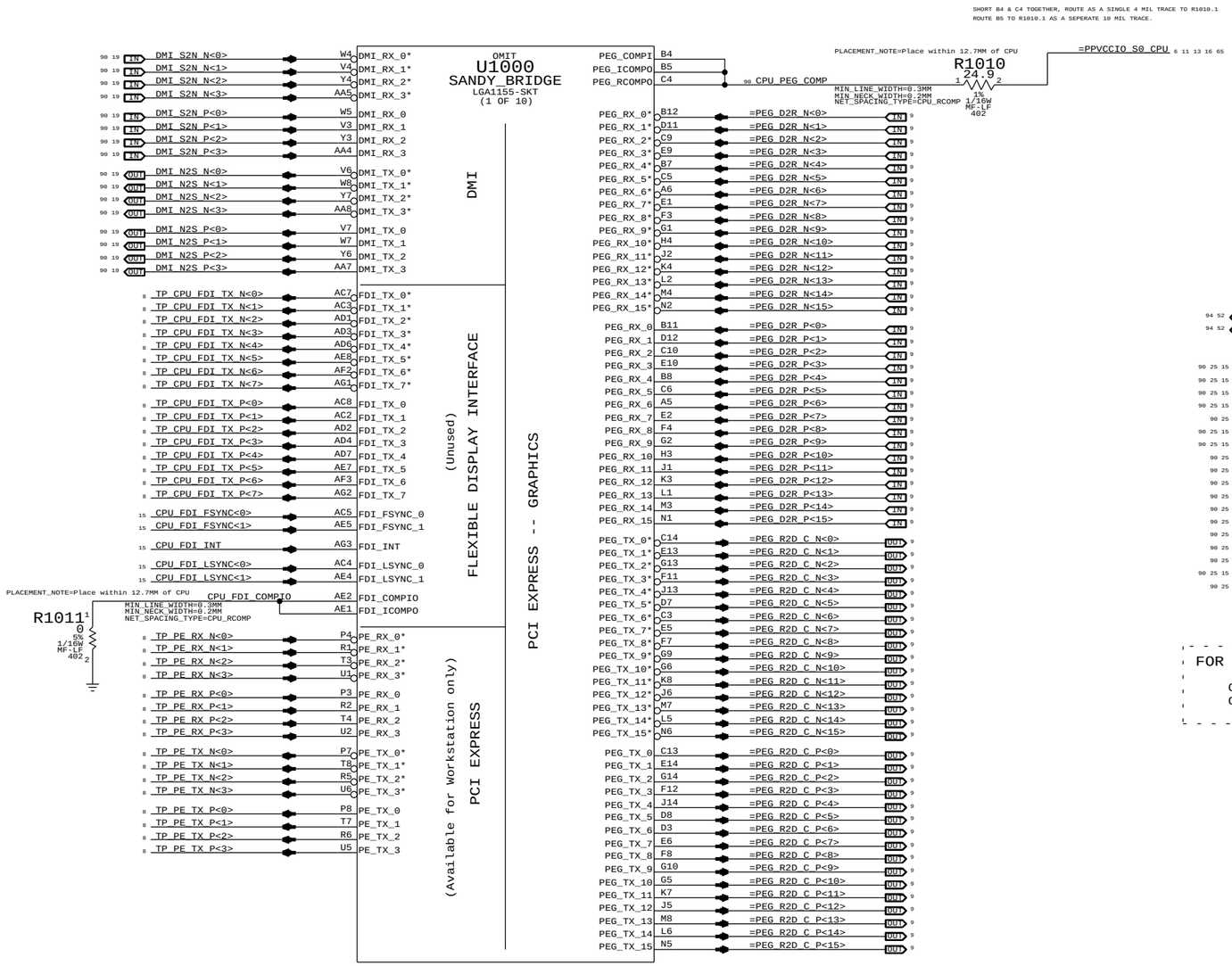

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

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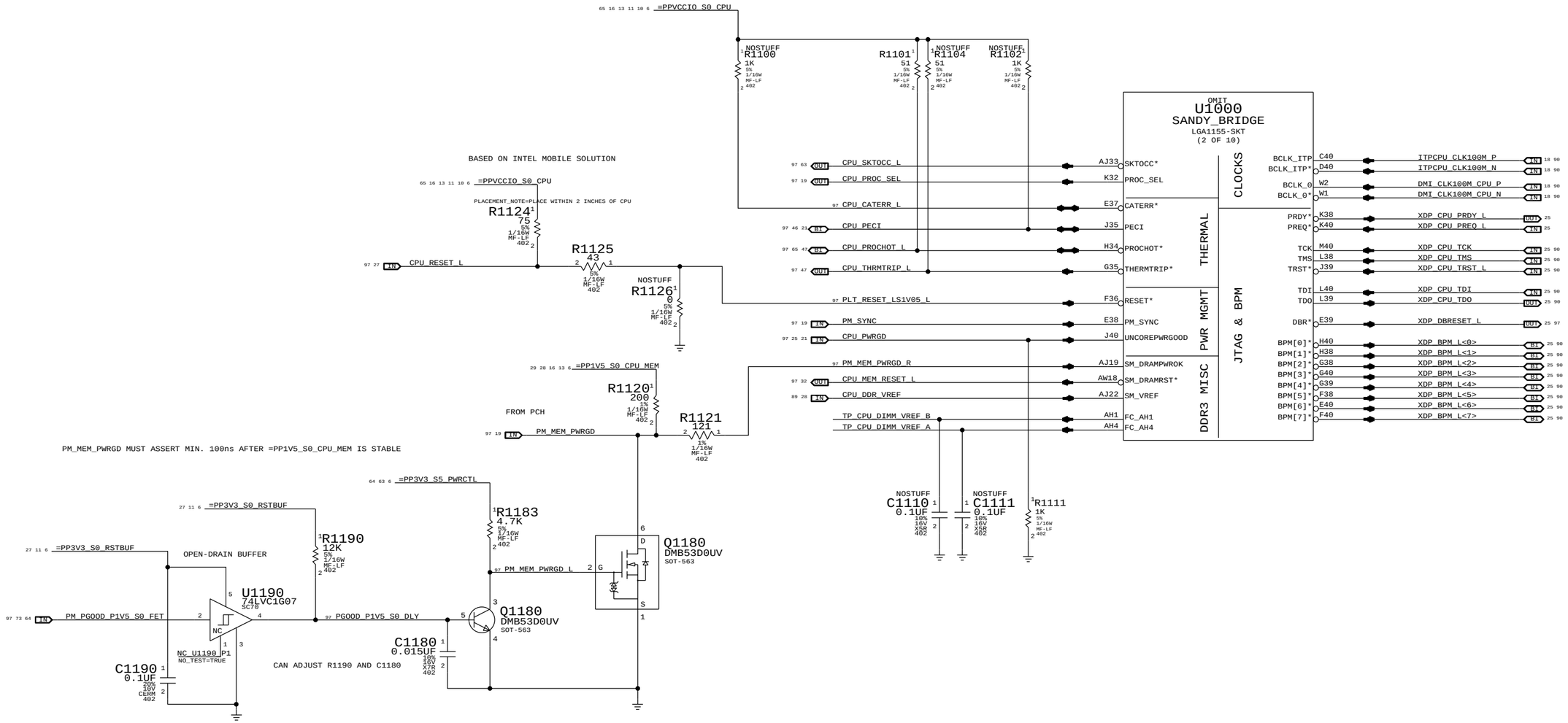

PAGE TITLE	CPU CLOCK/MISC/JTAG
	Apple Inc.
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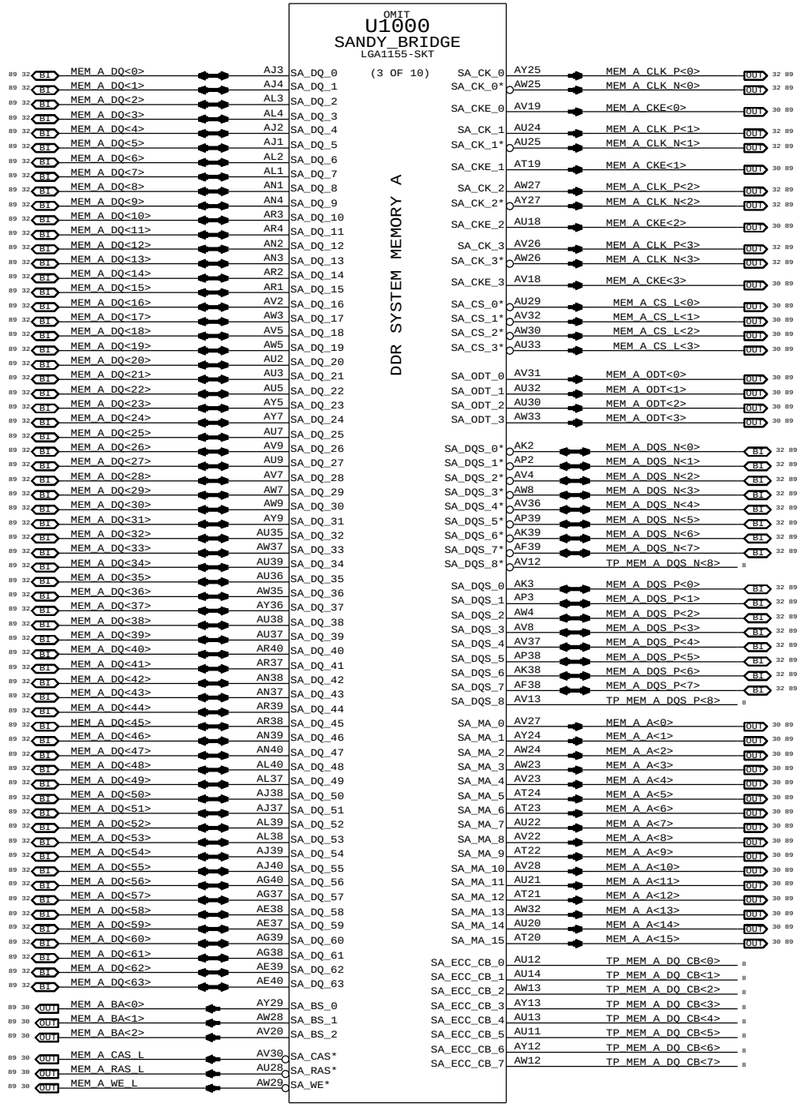

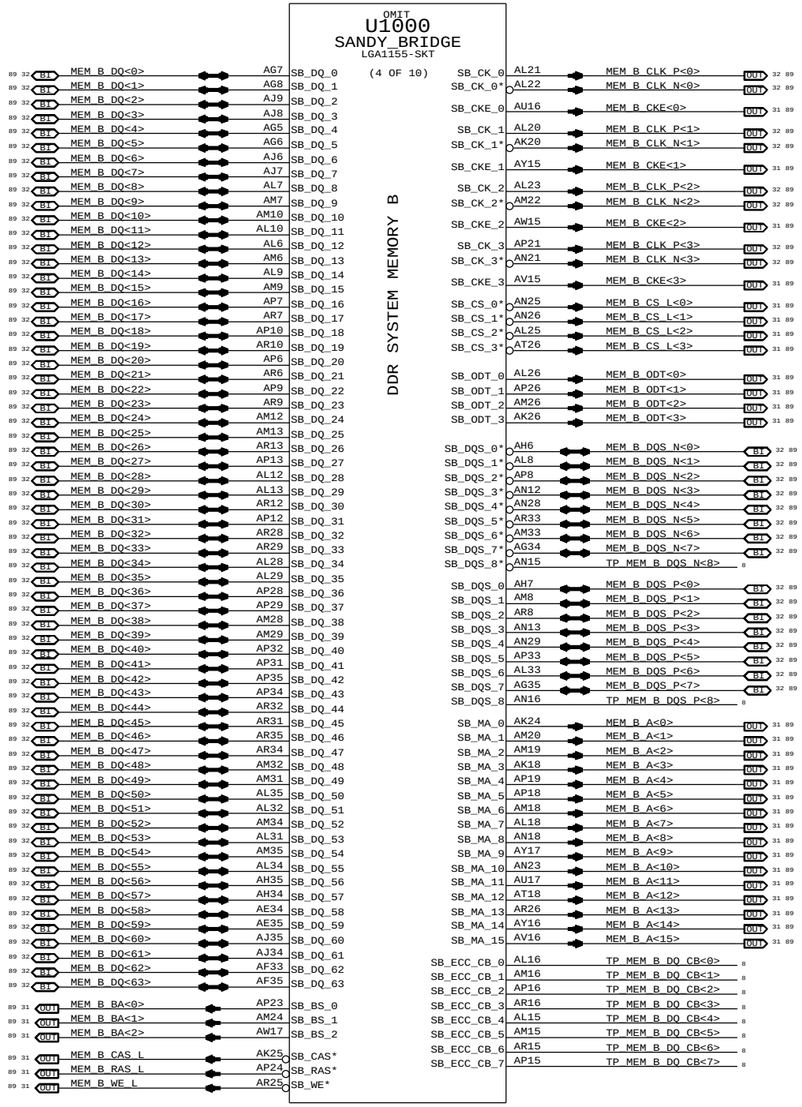

SYNC DATE=01/06/2011

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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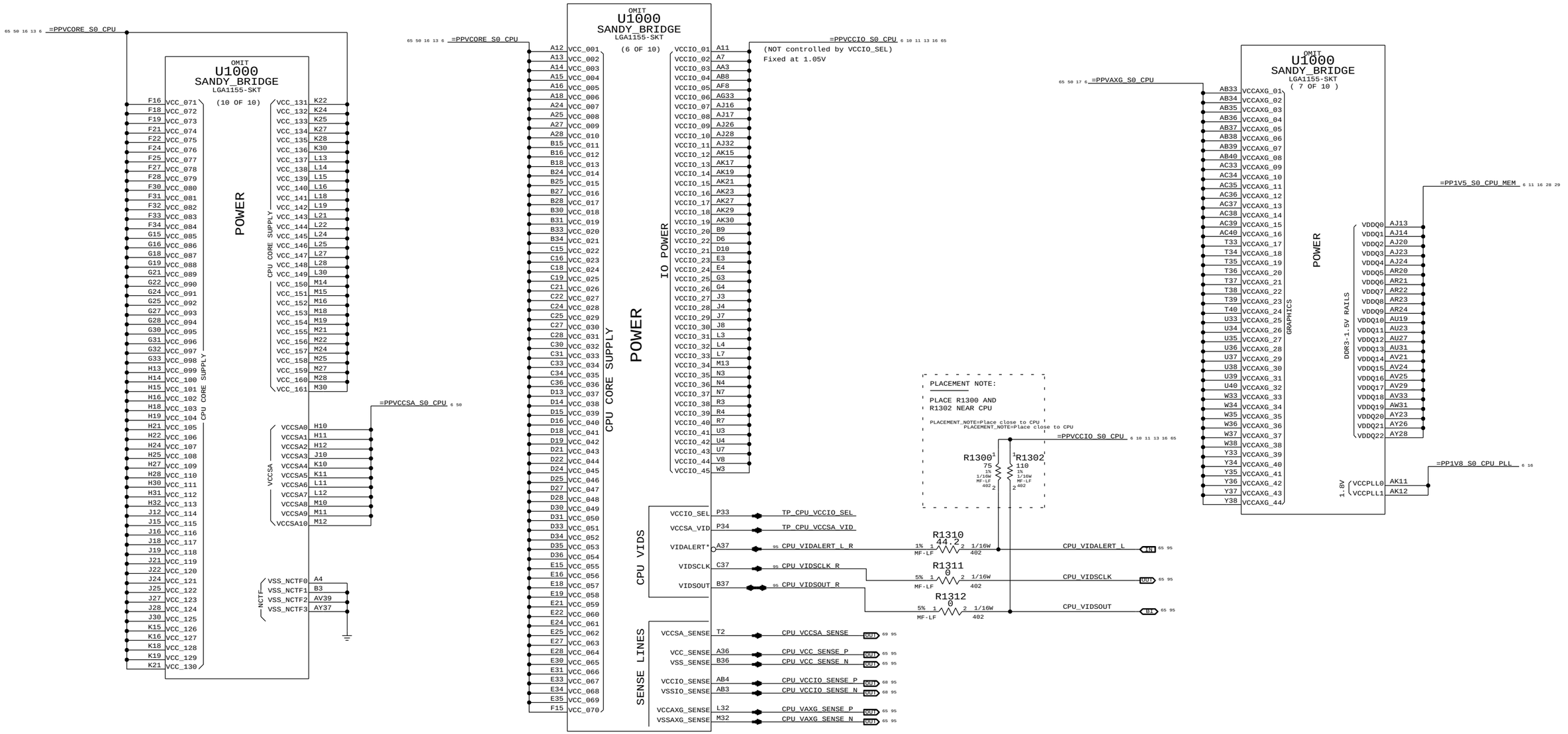

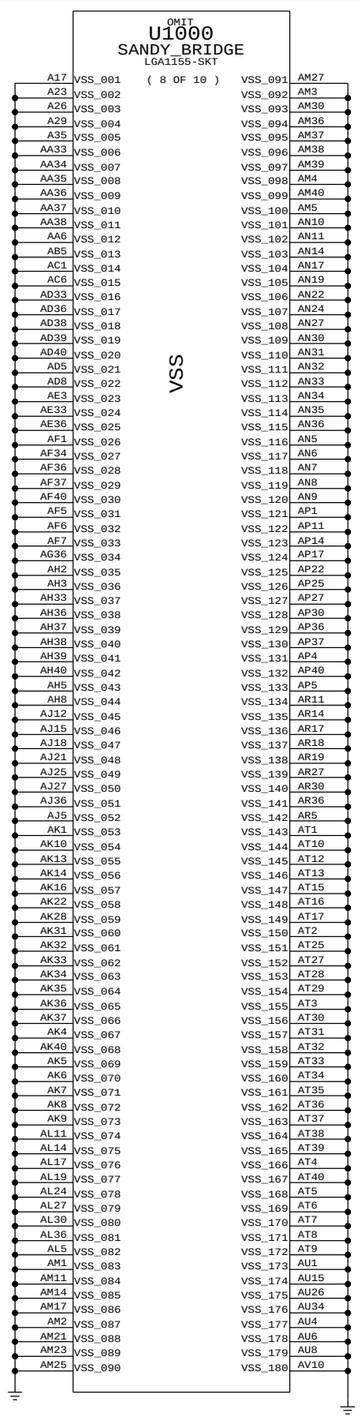

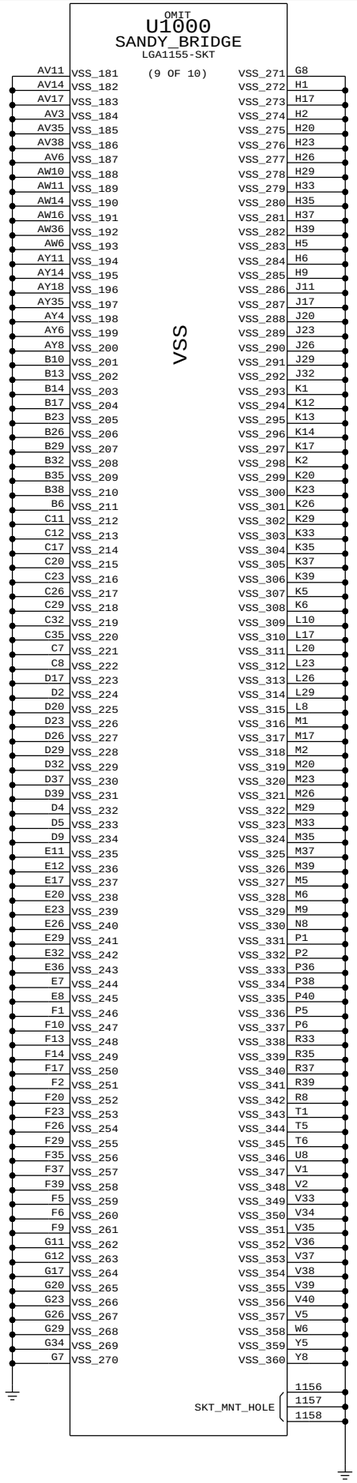

PAGE TITLE
CPU GROUNDS

Apple Inc.

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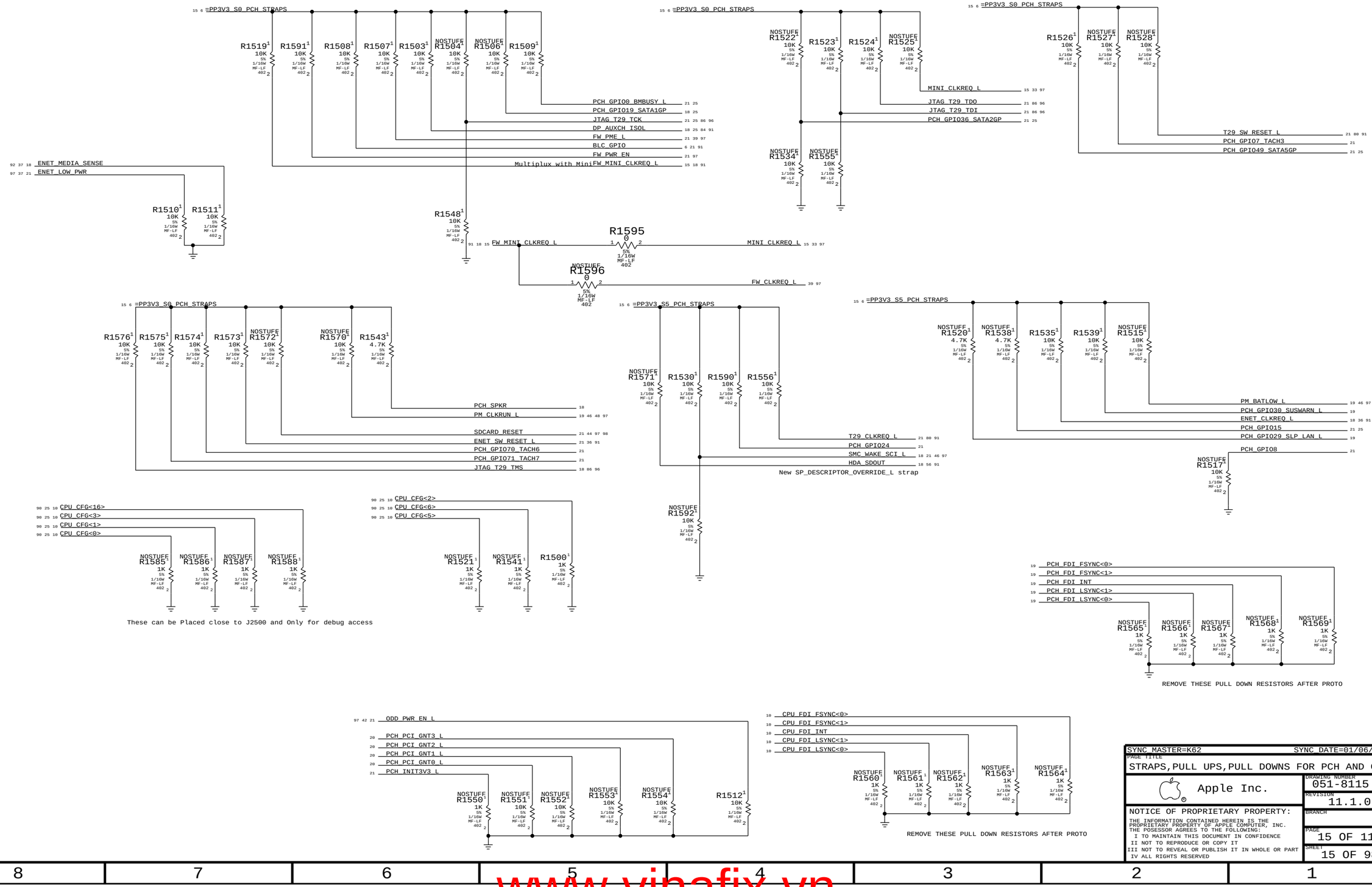

CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

16 13 6 =PPVCORE_S0_CPU
65 50

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

C1600 22UF 20% 6.3V CERM-X5R 805-3
C1601 22UF 20% 6.3V CERM-X5R 805-3
C1602 22UF 20% 6.3V CERM-X5R 805-3
C1603 22UF 20% 6.3V CERM-X5R 805-3
C1604 22UF 20% 6.3V CERM-X5R 805-3
C1605 22UF 20% 6.3V CERM-X5R 805-3
C1606 22UF 20% 6.3V CERM-X5R 805-3
C1607 22UF 20% 6.3V CERM-X5R 805-3
C1608 22UF 20% 6.3V CERM-X5R 805-3
C1609 22UF 20% 6.3V CERM-X5R 805-3

C1610 22UF 20% 6.3V CERM-X5R 805-3
C1611 22UF 20% 6.3V CERM-X5R 805-3
C1612 22UF 20% 6.3V CERM-X5R 805-3
C1613 22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 72

65 50 16 13 6 =PPVCORE_S0_CPU

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

C1620 10UF 20% 16V X5R 603
C1621 10UF 20% 16V X5R 603
C1622 10UF 20% 16V X5R 603
C1623 10UF 20% 16V X5R 603
C1624 10UF 20% 16V X5R 603
C1625 10UF 20% 16V X5R 603
C1626 10UF 20% 16V X5R 603
C1627 10UF 20% 16V X5R 603
C1628 10UF 20% 16V X5R 603
C1629 10UF 20% 16V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 6s =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

C1650 22UF 20% 6.3V CERM-X5R 805
C1651 22UF 20% 6.3V CERM-X5R 805
C1652 22UF 20% 6.3V CERM-X5R 805
C1653 22UF 20% 6.3V CERM-X5R 805
C1654 22UF 20% 6.3V CERM-X5R 805
C1655 22UF 20% 6.3V CERM-X5R 805
C1656 22UF 20% 6.3V CERM-X5R 805
C1657 22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 22uF 20% 6.3V CERM-X5R 805
C1677 22uF 20% 6.3V CERM-X5R 805
C1678 22uF 20% 6.3V CERM-X5R 805
C1679 22uF 20% 6.3V CERM-X5R 805
C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 1UF 10% 10V X5R 402
C1683 1UF 10% 10V X5R 402
C1684 1UF 10% 16V X5R 402
C1685 1UF 10% 16V X5R 402
C1686 1UF 10% 16V X5R 402

Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V CERM-X5R 805
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

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CPU NON-GFX DECOUPLING

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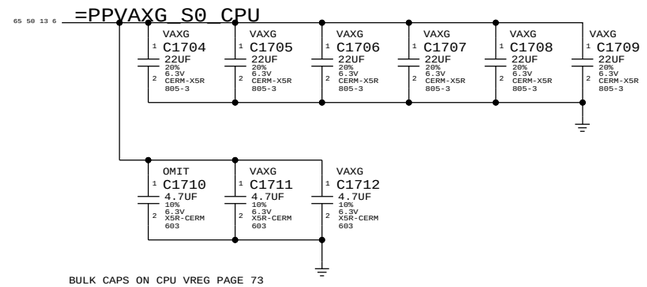
VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

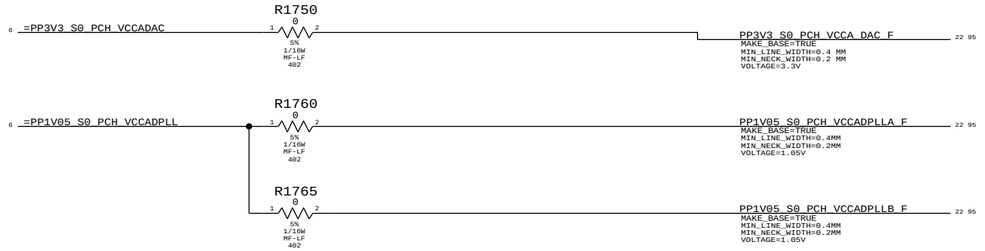
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

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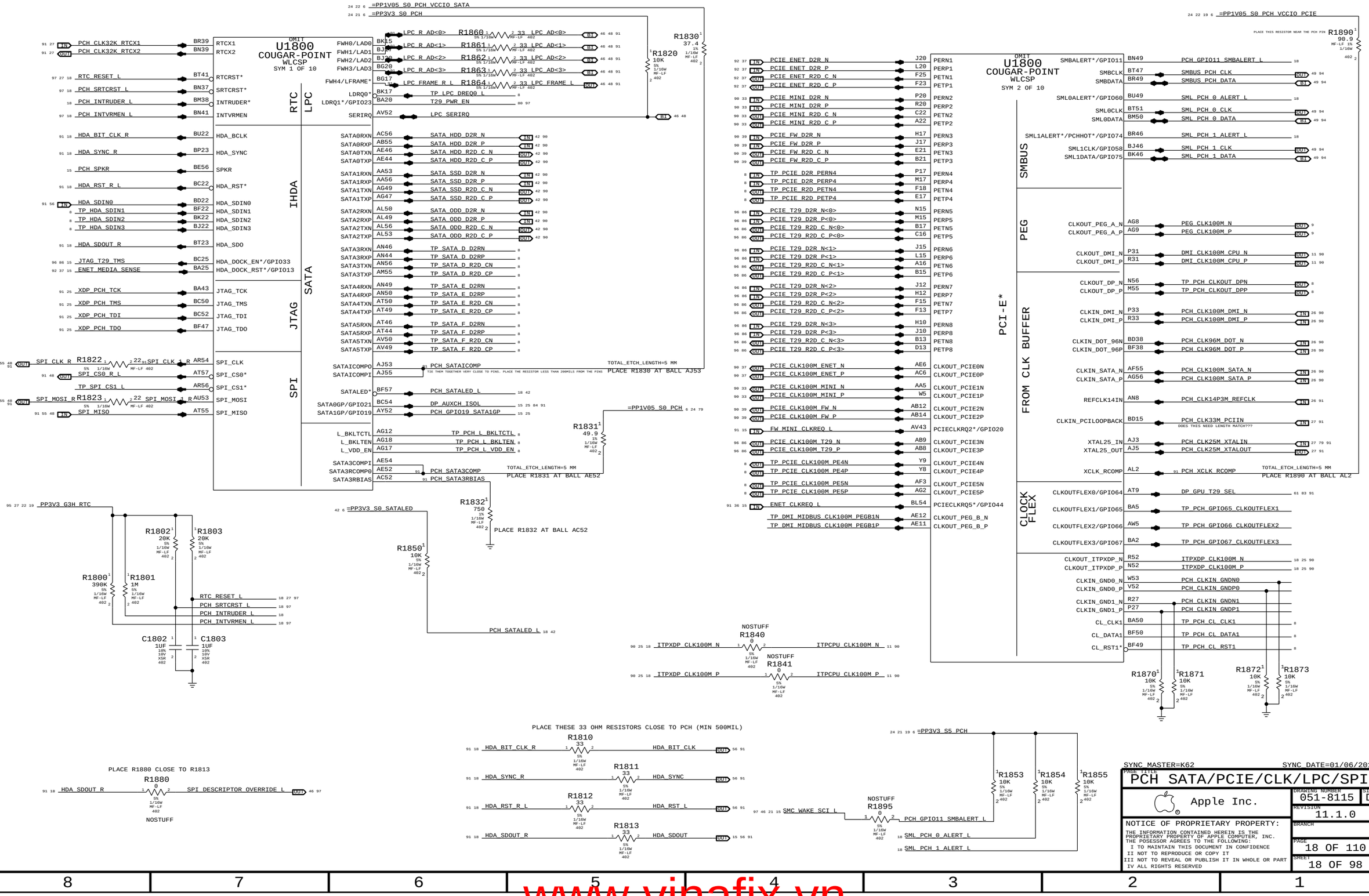

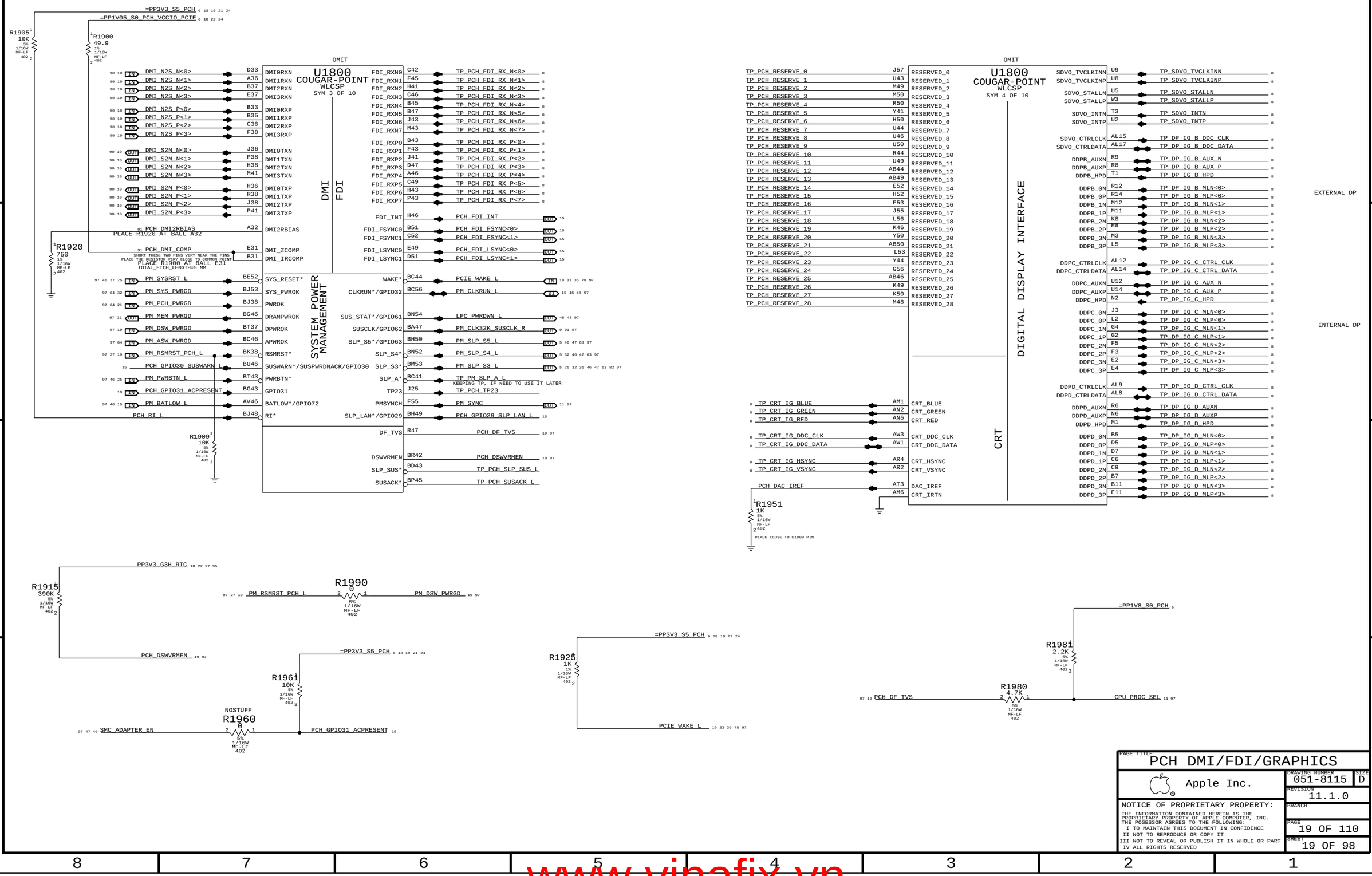

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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COUGAR-POINT
WLCSP
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PCI

TP_PCI_AD<0>	BF15	AD0	
TP_PCI_AD<1>	BF17	AD1	
TP_PCI_AD<2>	BT7	AD2	
TP_PCI_AD<3>	BT13	AD3	
TP_PCI_AD<4>	BG12	AD4	
TP_PCI_AD<5>	BN11	AD5	
TP_PCI_AD<6>	BJ12	AD6	
TP_PCI_AD<7>	BU9	AD7	
TP_PCI_AD<8>	BR12	AD8	
TP_PCI_AD<9>	BJ3	AD9	
TP_PCI_AD<10>	BR9	AD10	
TP_PCI_AD<11>	BJ10	AD11	
TP_PCI_AD<12>	BM8	AD12	
TP_PCI_AD<13>	BF3	AD13	
TP_PCI_AD<14>	BN2	AD14	
TP_PCI_AD<15>	BE4	AD15	
TP_PCI_AD<16>	BE6	AD16	
TP_PCI_AD<17>	BG15	AD17	
TP_PCI_AD<18>	BC6	AD18	
TP_PCI_AD<19>	BT11	AD19	
TP_PCI_AD<20>	BA14	AD20	
TP_PCI_AD<21>	BL2	AD21	
TP_PCI_AD<22>	BC4	AD22	
TP_PCI_AD<23>	BL4	AD23	
TP_PCI_AD<24>	BC2	AD24	
TP_PCI_AD<25>	BM13	AD25	
TP_PCI_AD<26>	BA9	AD26	
TP_PCI_AD<27>	BF9	AD27	
TP_PCI_AD<28>	BA8	AD28	
TP_PCI_AD<29>	BF8	AD29	
TP_PCI_AD<30>	AV17	AD30	
TP_PCI_AD<31>	BK12	AD31	
TP_PCI_C_BE_L<0>	BN4	C/BE0*	
TP_PCI_C_BE_L<1>	BP7	C/BE1*	
TP_PCI_C_BE_L<2>	BG2	C/BE2*	
TP_PCI_C_BE_L<3>	BP13	C/BE3*	
PCI_INTA_L	BK10	PIRQA*	
PCI_INTB_L	BJ5	PIRQB*	
PCI_INTC_L	BM15	PIRQC*	
PCI_INTD_L	BP5	PIRQD*	
PCH_PCI_GNT0_L	BA15	GNT0*	
PCH_PCI_GNT1_L	AV8	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BU12	GNT2*/GPIO53	
PCH_PCI_GNT3_L	BE2	GNT3*/GPIO55	
PCI_SERR_L	BR6	SERR*	
PCI_PERR_L	BM3	PERR*	
PCI_IRDY_L	BF11	IRDY*	
TP_PCI_PAR	BH8	PAR	
PCI_DEVSEL_L	BH9	DEVSEL*	
PCI_FRAME_L	BC11	FRAME*	
PCI_PLOCK_L	BA17	PLOCK*	
PCI_STOP_L	BC12	STOP*	
PCI_TRDY_L	BC8	TRDY*	
TP_PCI_PME_L	AV15	PME*	
PLT_RESET_L (OUT)	BK48	PLTRST*	
LPC_CLK33M_SMC_R (OUT)	AT11	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R (OUT)	AN14	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AT12	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AT17	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT (OUT)	AT14	CLKOUT_PCI4	

USB

USBP0N	BF36	USB_HUB1_UP_N	USB HUB 1
USBP0P	BD36	USB_HUB1_UP_P	
USBP1N	BC33	TP_USB_1N	Unused
USBP1P	BA33	TP_USB_1P	
USBP2N	BM33	TP_USB_2N	Unused
USBP2P	BM35	TP_USB_2P	
USBP3N	BT33	TP_USB_3N	Unused
USBP3P	BU32	TP_USB_3P	
USBP4N	BR32	TP_USB_4N	Unused
USBP4P	BT31	TP_USB_4P	
USBP5N	BN29	TP_USB_5N	Unused
USBP5P	BM30	TP_USB_5P	
USBP6N	BK33	TP_USB_6N	Unused
USBP6P	BJ33	TP_USB_6P	
USBP7N	BF31	TP_USB_7N	Unused
USBP7P	BD31	TP_USB_7P	
USBP8N	BN27	USB_HUB2_UP_N	USB HUB 2
USBP8P	BR29	USB_HUB2_UP_P	
USBP9N	BR26	USB_CAMERA_N	USB CAMERA
USBP9P	BT27	USB_CAMERA_P	
USBP10N	BK25	TP_USB_10N	Unused
USBP10P	BJ25	TP_USB_10P	
USBP11N	BJ31	TP_USB_11N	Unused
USBP11P	BK31	TP_USB_11P	
USBP12N	BF27	TP_USB_12N	Unused
USBP12P	BD27	TP_USB_12P	
USBP13N	BJ27	TP_USB_13N	Unused
USBP13P	BK27	TP_USB_13P	
USBRBIAS*	BP25	PCH_USB_RBIAS	
USBRBIAS	BM25		

PLACE THE RESISTOR CLOSE TO COMMON POINT
TIE TRACES TOGETHER CLOSE TO PIN

OC0*/GPIO59	BM43	
OC1*/GPIO40	BD41	
OC2*/GPIO41	BG41	
OC3*/GPIO42	BK43	
OC4*/GPIO43	BP43	
OC5*/GPIO9	BJ41	
OC6*/GPIO10	BT45	
OC7*/GPIO14	BM45	

R2010	10K	PCI_INTA_L
R2011	10K	PCI_INTB_L
R2012	10K	PCI_INTC_L
R2013	10K	PCI_INTD_L
R2015	10K	PCI_REQ0_L
R2016	10K	PCI_REQ1_L
		PCI_REQ2_L
		PCI_REQ3_L
R2030	10K	USE_HDD_OOB_L
R2031	10K	T29_MCU_INT_L
		AUD_IP_PERIPHERAL_DET
		AUD_I2C_INT_L
R2020	10K	PCI_SERR_L
R2021	10K	PCI_PERR_L
R2022	10K	PCI_IRDY_L
R2023	10K	PCI_DEVSEL_L
R2024	10K	PCI_FRAME_L
R2027	10K	PCI_PLOCK_L
R2025	10K	PCI_STOP_L
R2026	10K	PCI_TRDY_L

All: 5% 1/16W MF-LF 402

R2061	10K	5% 1/16W MF-LF 402	
R2063	10K	5% 1/16W MF-LF 402	
R2065	10K	5% 1/16W MF-LF 402	PRODUCTION
R2068	10K	5% 1/16W MF-LF 402	
R2060	10K	5% 1/16W MF-LF 402	
R2062	10K	5% 1/16W MF-LF 402	
R2064	10K	5% 1/16W MF-LF 402	
R2066	10K	5% 1/16W MF-LF 402	

=PP3V3_S5_PCH_GPIO

R2070 22.6 1% 1/16W MF-LF 402
PLACE R2070 AT BALL BM25

=PP3V3_S0_PCH_GPIO

PCH SATA PORT 1 OPTION SELECT IS ODD OR SSD

PCI_REQ2_L — R2017 10K ODD_SATA:P2 — =PP3V3_S0_PCH_GPIO
R2098 10K ODD_SATA:P1

K60E MLB CFG SELECT

PCI_REQ3_L — R2018 10K T29 — =PP3V3_S0_PCH_GPIO
R2099 10K NO_T29

AP_PWR_EN	25 33 97
USB_HUB_SOFT_RESET_L	25 34 97
T29_DP_PORTA_PWR_EN	25 82 91 97
ENET_PWR_EN	25 36 97
T29_DP_PORTB_PWR_EN	25 91
SDCONN_STATE_CHANGE	25 45 97
PCH_GPIO10_OC6_L	25
PCH_GPIO14_OC7_L	25

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: PCH PCI/FLASHCACHE/USB

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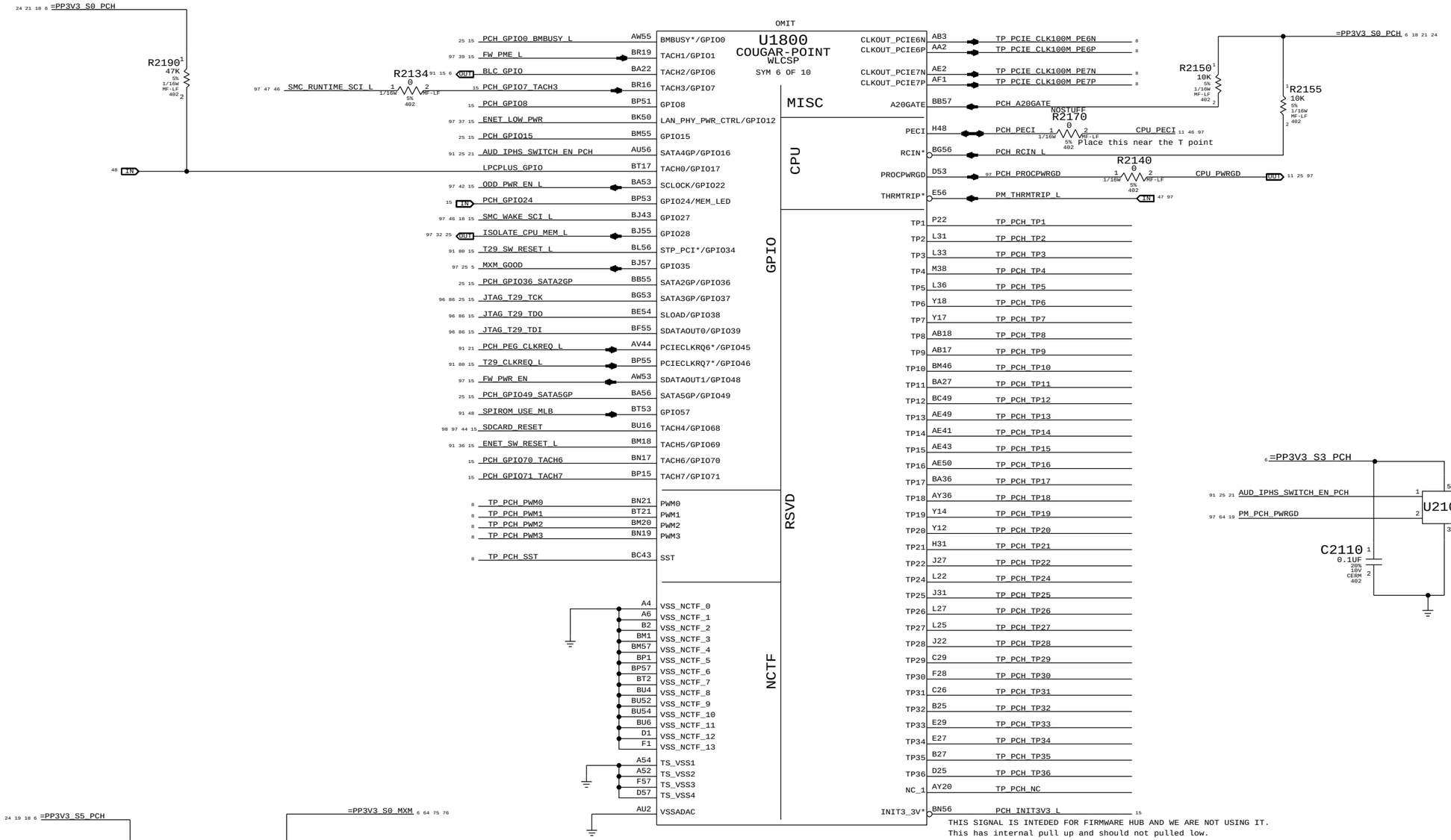

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: PCH MISC

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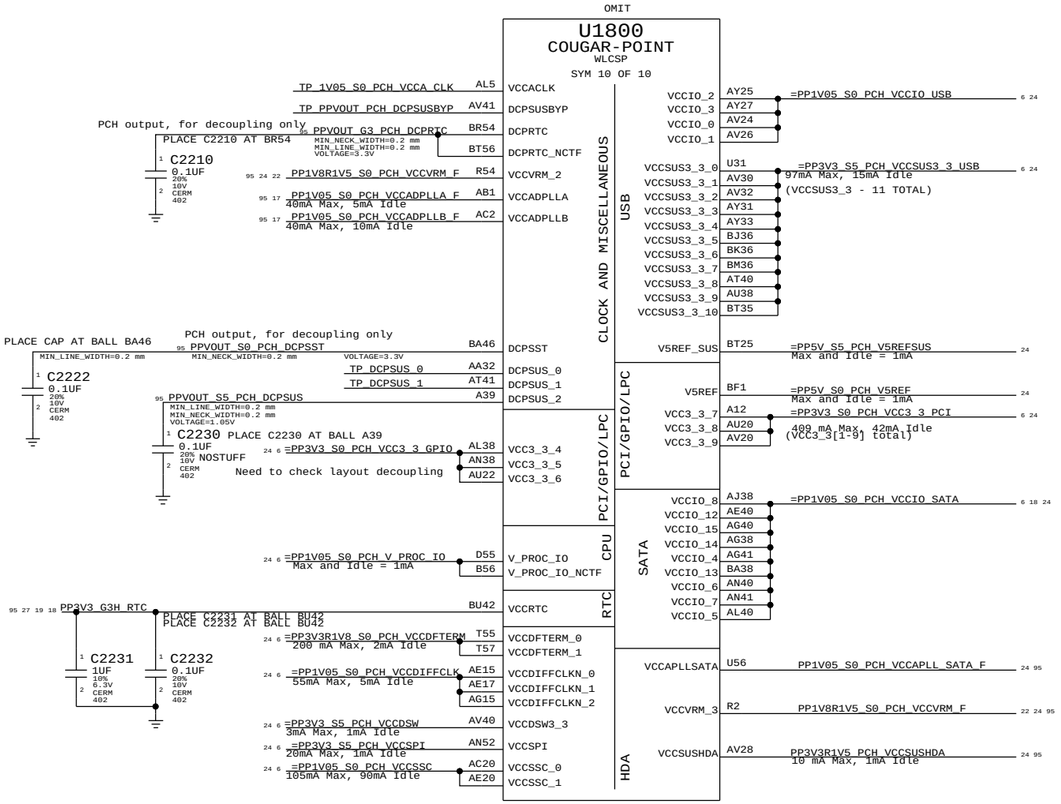

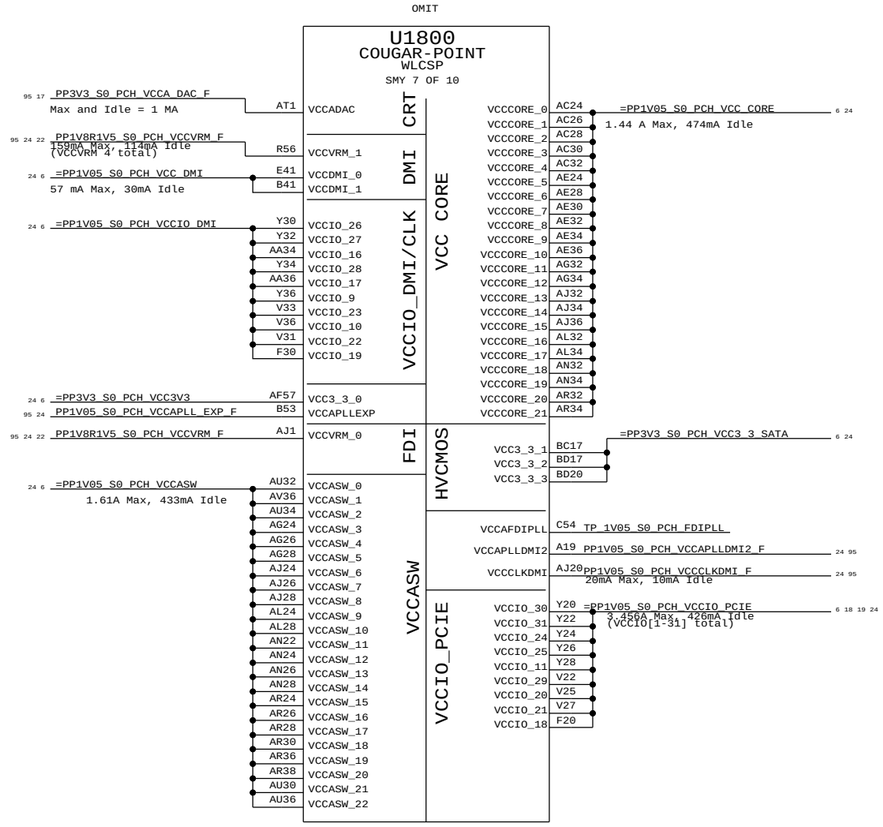

PAGE TITLE: PCH POWER

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BR36			AN15
C12			AN17
AY22			AN18
A26			AN20
A29			AN30
A42			AN36
A49			AN4
A9			AN43
AA20			AN47
AA22			AN54
AA24			AN9
AA26			AR20
AA28			AR22
AA30			AR52
AA38			AR6
AB11			AT15
AB15			AT18
AB40			AT43
AB41			AT47
AB43			AT52
AB47			AT6
AB52			AT8
AB57			AU24
AB6			AU26
AC22			AU28
AC34			AU5
AC36			AV12
AC38			AV18
AC4			AV22
AC54			AV34
AE14			AV38
AE18			AV47
AE22			AV6
AE26			AW57
AE38			AY38
AE4			AY6
AE47			B23
AE8	VSS	VSS	BA11
AE9			BA12
AF52			BA31
AF6			BA41
AG11			BA44
AG14			BA49
AG20			BB1
AG22			BB3
AG30			BB52
AG36			BB6
AG43			BC14
AG44			BC15
AG46			BC20
AG5			BC27
AG50			BC31
AG53			BC36
AH52			BC38
AH6			BC47
AJ22			BC9
AJ30			BD25
AJ57			BD33
AK52			BF12
AK6			BF20
AL11			BF25
AL18			BF33
AL20			BF41
AL22			BF43
AL26			BF46
AL30			BF52
AL36			BF6
AL41			BG22
AL46			BG25
AL47			BG27
AM3			BG31
AM52			BG33
AM57			BG36
AN11			

OMIT

U1800
COUGAR-POINT
WLCSP
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BG38			J46
BH52			J48
BH6			J5
BJ1			J53
BJ15			K52
BK20			K6
BK41			K9
BK52			L12
BK6			L17
BM10			L38
BM12			L41
BM16			L43
BM22			M20
BM23			M22
BM26			M25
BM28			M27
BM32			M31
BM40			M33
BM42			M36
BM48			M46
BM5			M52
BN31			M57
BN47			M6
BN6			M8
BP3			M9
BP33			N4
BP35			N54
BR22			R11
BR52			R15
BU19			R17
BU26			R22
BU29			R4
BU36			R41
BU39			R43
C19			R46
C32			R49
C39			T52
C4			T6
D15			U11
D23	VSS	VSS	U15
D3			U17
D35			U20
D43			U22
D45			U25
E19			U27
E39			U33
E54			U36
E6			U38
E9			U41
F10			U47
F12			U53
F16			V20
F22			V38
F26			V6
F32			W1
F33			W55
F35			W57
F36			Y11
F40			Y15
F42			Y38
F46			Y40
F48			Y43
F50			Y46
F8			Y47
G54			Y49
H15			Y52
H20			Y6
H22			AL43
H25			AL44
H27			R36
H33			P36
H6			R25
J1			P25
J33			

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PCH GROUNDS

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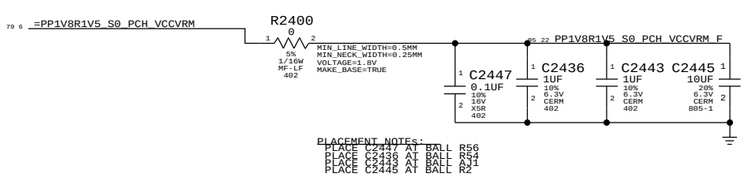
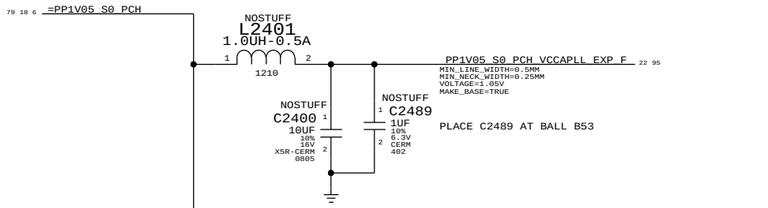
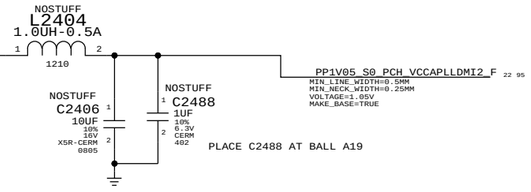
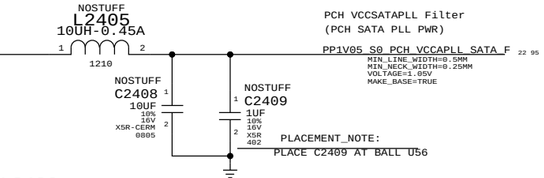
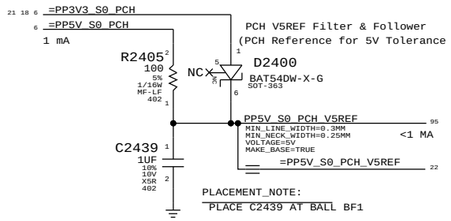
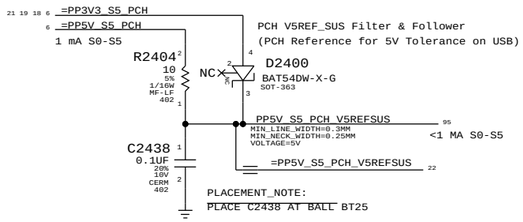


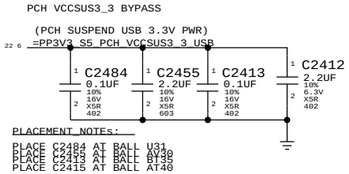


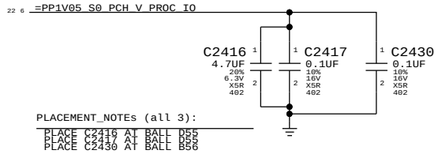




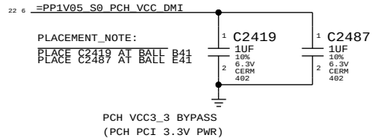


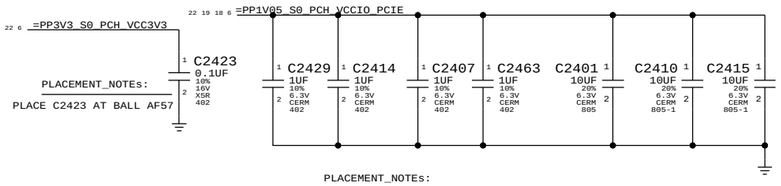


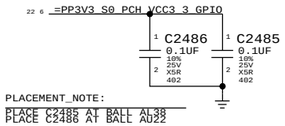


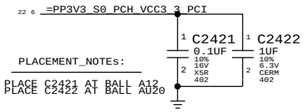


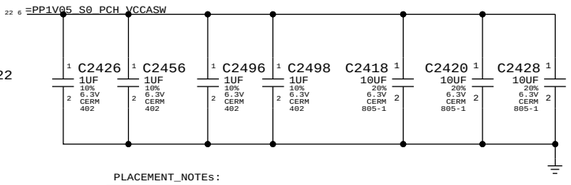
PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)

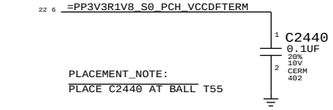




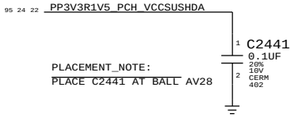


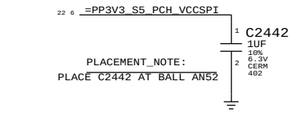


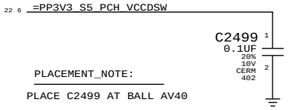


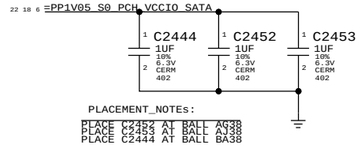


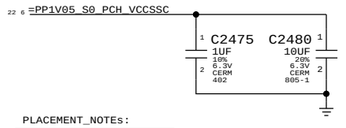
PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)

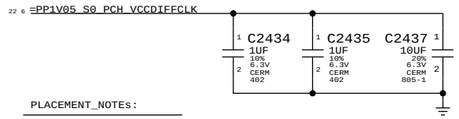




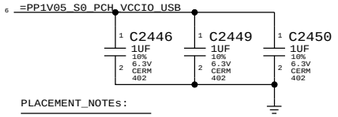


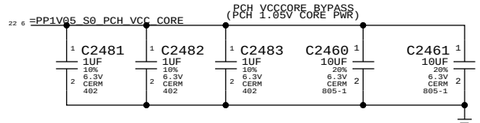


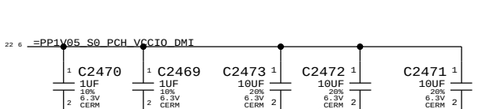


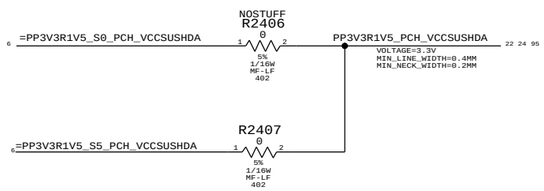


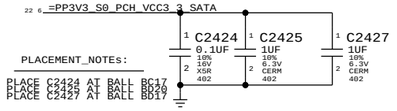
PCH VCCIO BYPASS
(PCH USB 1.05V PWR)











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PROCESSOR MINI XDP

PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs

XDP_CPU_BPM
RP2500
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>

XDP_CPU_CFG
RP2501
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

PLACEMENT_NOTE=Place close to CPU
XDP R2500 1K
CPU_PWRGD

PLACEMENT_NOTE=Place close to SMC
XDP R2502 0
PM_PWRBTN_L

PLACEMENT_NOTE=Place close to CPU
XDP R2501 1K
CPU_CFG<0>

XDP R2504 0
PM_PGOOD_PVCORE_CPU

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<16> CPU_CFG<17> CPU_CFG<0> CPU_CFG<1> CPU_CFG<2> CPU_CFG<3> CPU_CFG<8> CPU_CFG<9> CPU_CFG<4> CPU_CFG<5> CPU_CFG<6> CPU_CFG<7>

XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
XDP_DBRESET_L
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS

XDP C2500 0.1uF
XDP C2501 0.1uF

XDP R2515 0 PLACEMENT_NOTE=Place close to R1841 ITPXDP_CLK100M_P
XDP R2516 0 PLACEMENT_NOTE=Place close to R1840 ITPXDP_CLK100M_N

<- 1K SERIES R ON PCH SUPPORT P. 28

NOTE: XDP_DBRESET_L pulled-up to 3.3V on P. 28

PLACEMENT_NOTE=Place close to SW2800
XDP R2506 0
XDP_DBRESET_L
To Reset Button
PM_SYSRST_L

DESIGN NOTE:
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
XDP R2510 51
XDP R2511 51
XDP R2512 51
PLACEMENT_NOTE=Place close to J2500
PLACEMENT_NOTE=Place close to CPU

XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TRST_L

XDP R2513 51
XDP R2514 51

PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU

PCH MINI XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP R2582 0 OC0#/GPIO59 AP_PWR_EN
XDP R2580 0 OC1#/GPIO40 USB_HUB_SOFT_RESET_L
XDP R2583 0 OC2#/GPIO41 T29_DP_PORTA_PWR_EN
XDP R2587 0 OC3#/GPIO42 ENET_PWR_EN
XDP R2586 0 OC4#/GPIO43 T29_DP_PORTB_PWR_EN
XDP R2581 0 OC5#/GPIO9 SDCONN_STATE_CHANGE
XDP R2584 1K =PP3V3_S5_XDP
XDP R2585 0 PM_PWRBTN_L

TP_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>
XDP_PCH_AP_PWR_EN
XDP_PCH_USB_HUB_SOFT_RST_L
XDP_PCH_T29_DP_PORTA_PWR_EN
XDP_PCH_ENET_PWR_EN
TP_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>
XDP_PCH_T29_DP_PORTB_PWR_EN
XDP_PCH_SDCONN_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

XDP_PCH_GPIO15
PCH_GPIO9_BMBUSY_L
XDP_PCH_ISOLATE_CPU_MEM_L
XDP_PCH_MXM_GOOD
XDP_PCH_DP_AUXCH_ISOL
PCH_GPIO19_SATA1GP
TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1>
PCH_GPIO36_SATA2GP
XDP_PCH_JTAG_T29_TCK
XDP_PCH_AUD_IPHS_SWITCH_EN
PCH_GPIO49_SATA5GP
TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5
XDP_PCH_TDO
TP_XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS
XDPPCH_PLTRST_L
XDP_DBRESET_L

XDP R2578 0 PLACEMENT_NOTE=Place close to PCH GPIO15 PCH_GPIO15
XDP R2576 0 PLACEMENT_NOTE=Place close to PCH MGPIO7/GPIO28 ISOLATE_CPU_MEM_L
XDP R2577 0 PLACEMENT_NOTE=Place close to PCH GPIO35 MXM_GOOD
XDP R2575 0 PLACEMENT_NOTE=Place close to PCH SATA0GP/GPIO21 DP_AUXCH_ISOL
XDP R2573 0 PLACEMENT_NOTE=Place close to PCH SATA3GP/GPIO37 JTAG_T29_TCK
XDP R2579 0 PLACEMENT_NOTE=Place close to PCH SATA4GP/GPIO16 AUD_IPHS_SWITCH_EN_PCH

SATA2GP/GPIO36

<- 1K SERIES R ON PCH SUPPORT P. 28

XDP C2580 0.1uF
XDP C2581 0.1uF

PLACEMENT NOTE:
PLACE TDO TERM NEAR PCH XDP CONN
XDP R2550 200
XDP R2551 200
XDP R2552 200
PLACEMENT_NOTE=Place close to J2550
PLACEMENT_NOTE=Place close to PCH

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK

XDP R2553 100
XDP R2554 100
XDP R2555 100
XDP R2556 51

This is to derive 1.05V SUS RAIL

PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH

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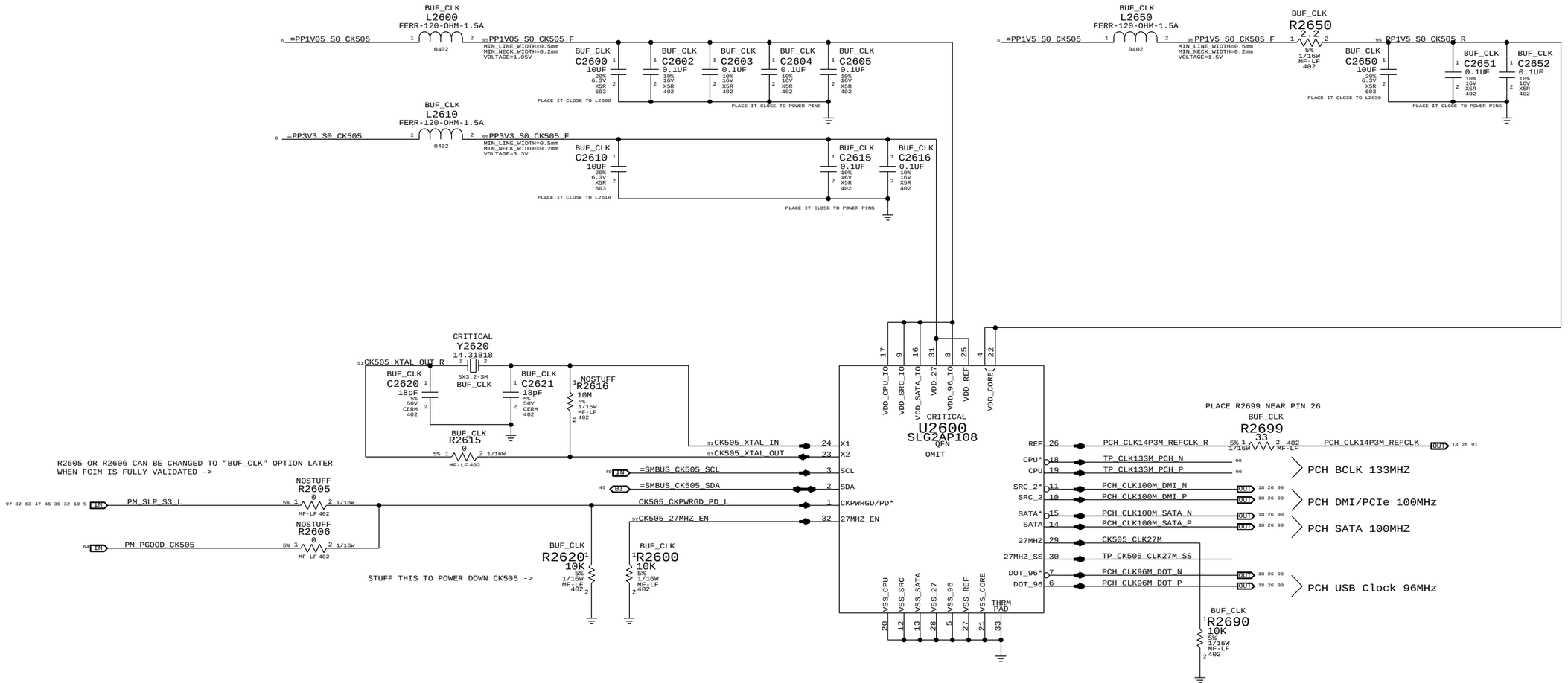
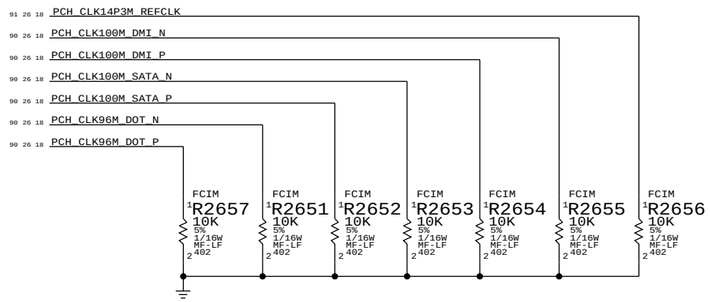


UNUSED clock terminations for FCIM MODE



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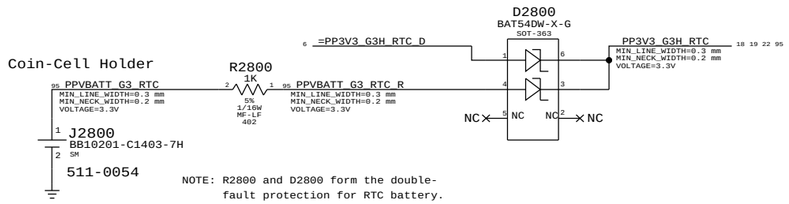
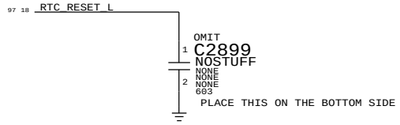
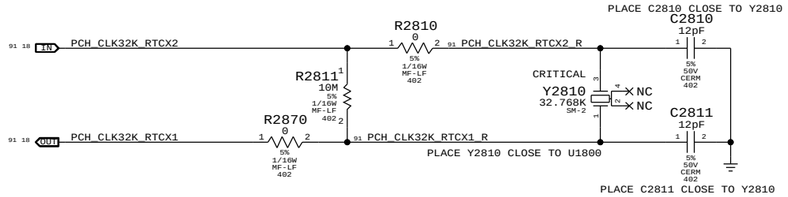
RTC Power Sources



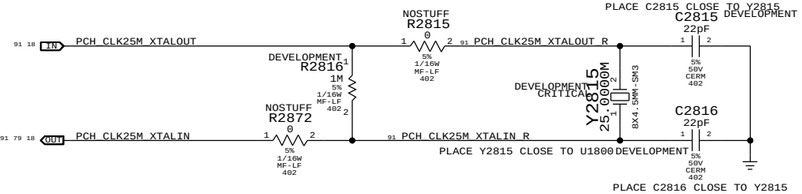
NOTE: R2800 and D2800 form the double-
fault protection for RTC battery.

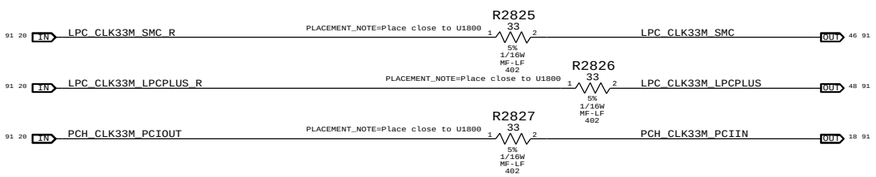


PCH RTC Crystal

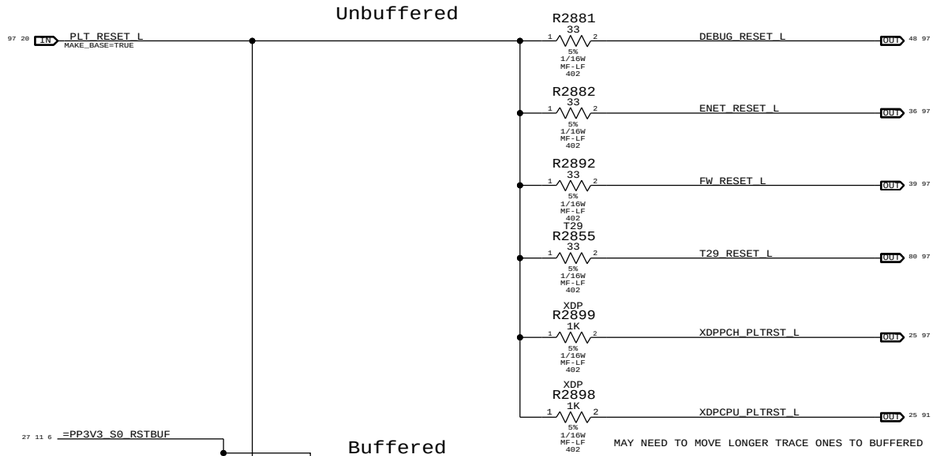


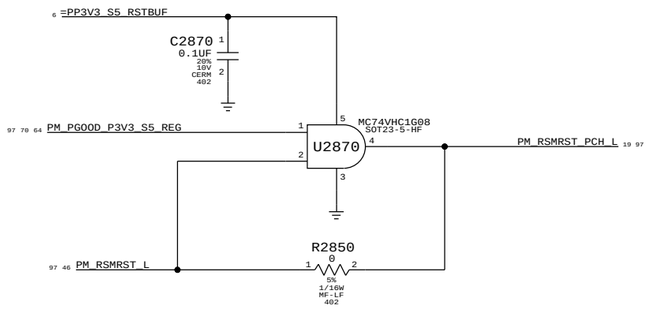
PCH 25MHZ CRYSTAL





Platform Reset Connections





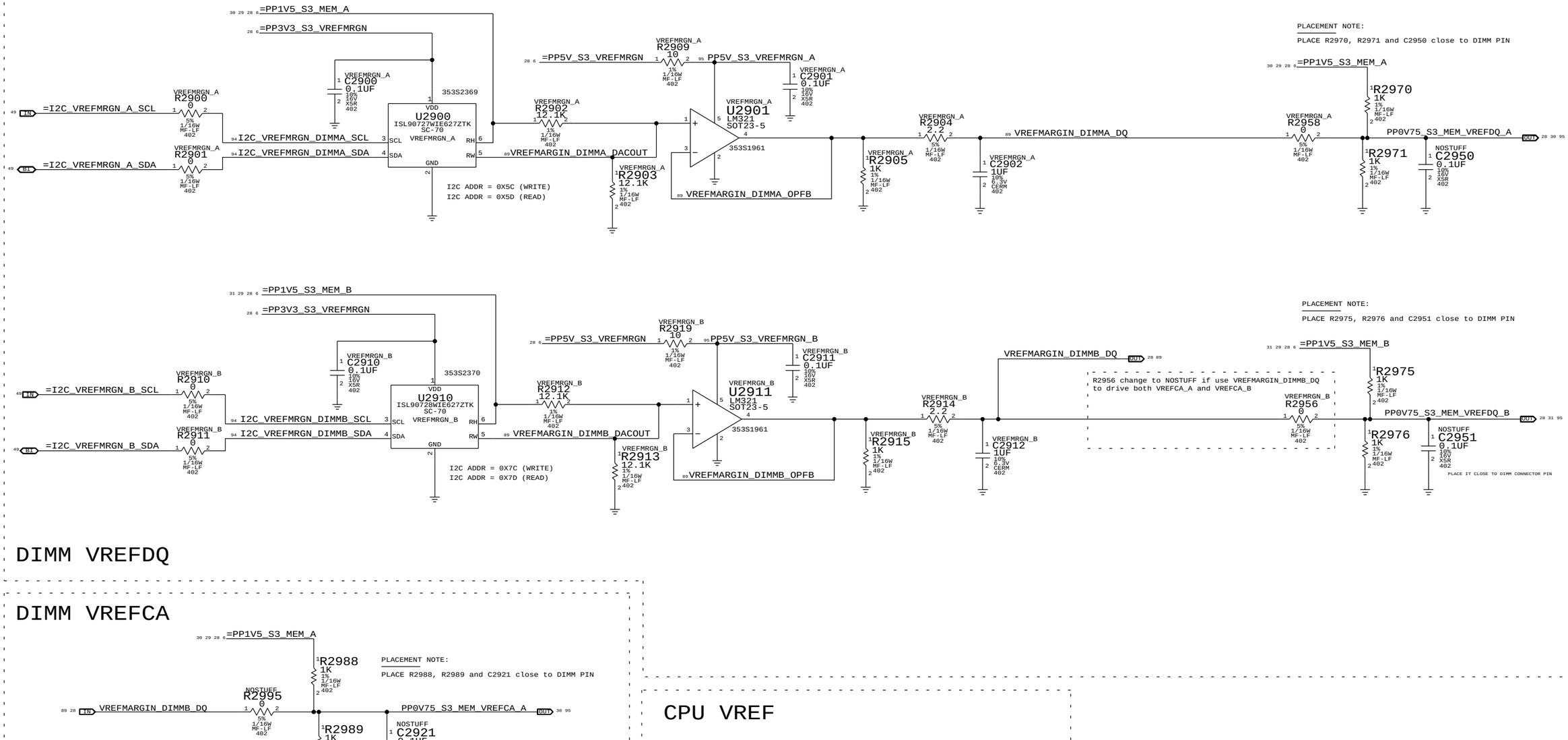
SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CHIPSET SUPPORT

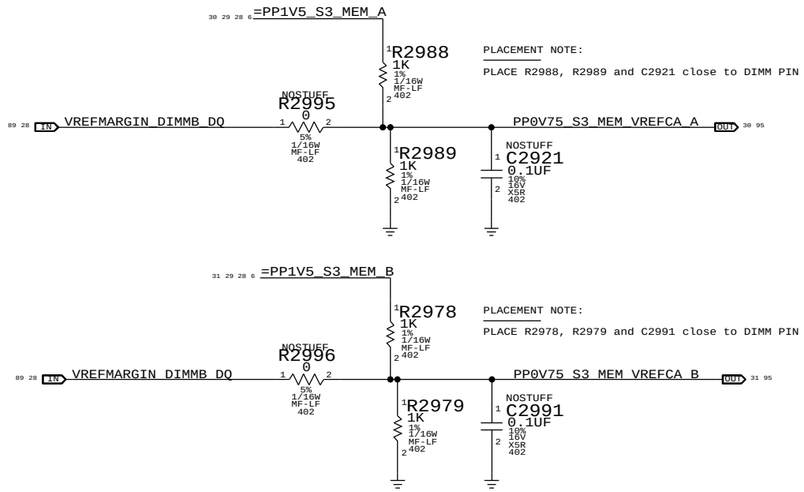
Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 28 OF 110
SHEET: 27 OF 98

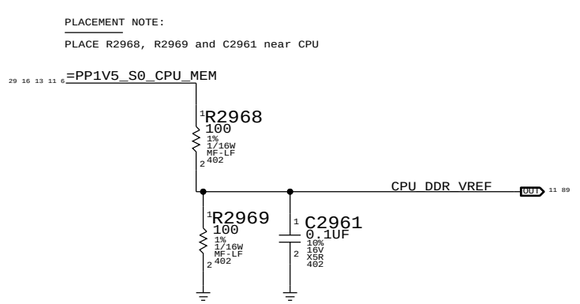


DIMM VREFDQ

DIMM VREFCA



CPU VREF



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 29 OF 110

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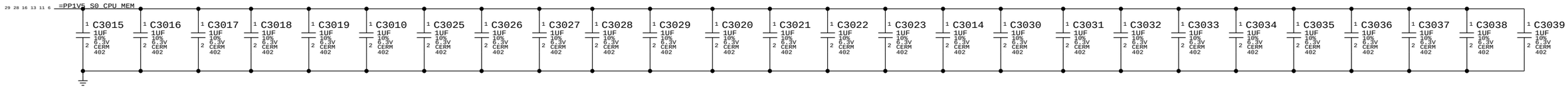
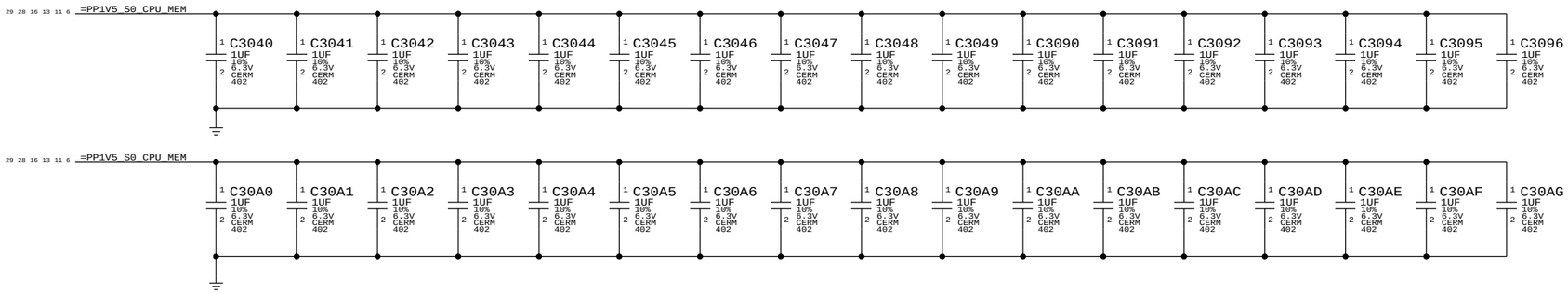
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

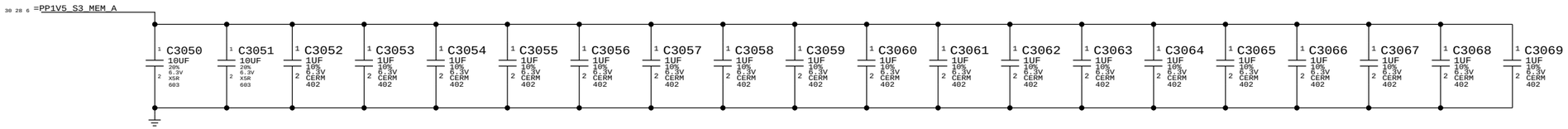
DIMM B (FURTHER FROM CPU)



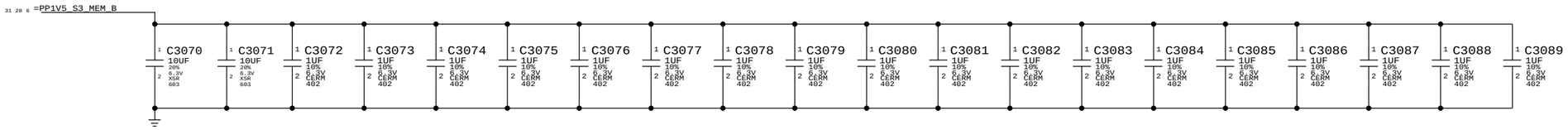
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: MEMORY CAPS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 30 OF 110

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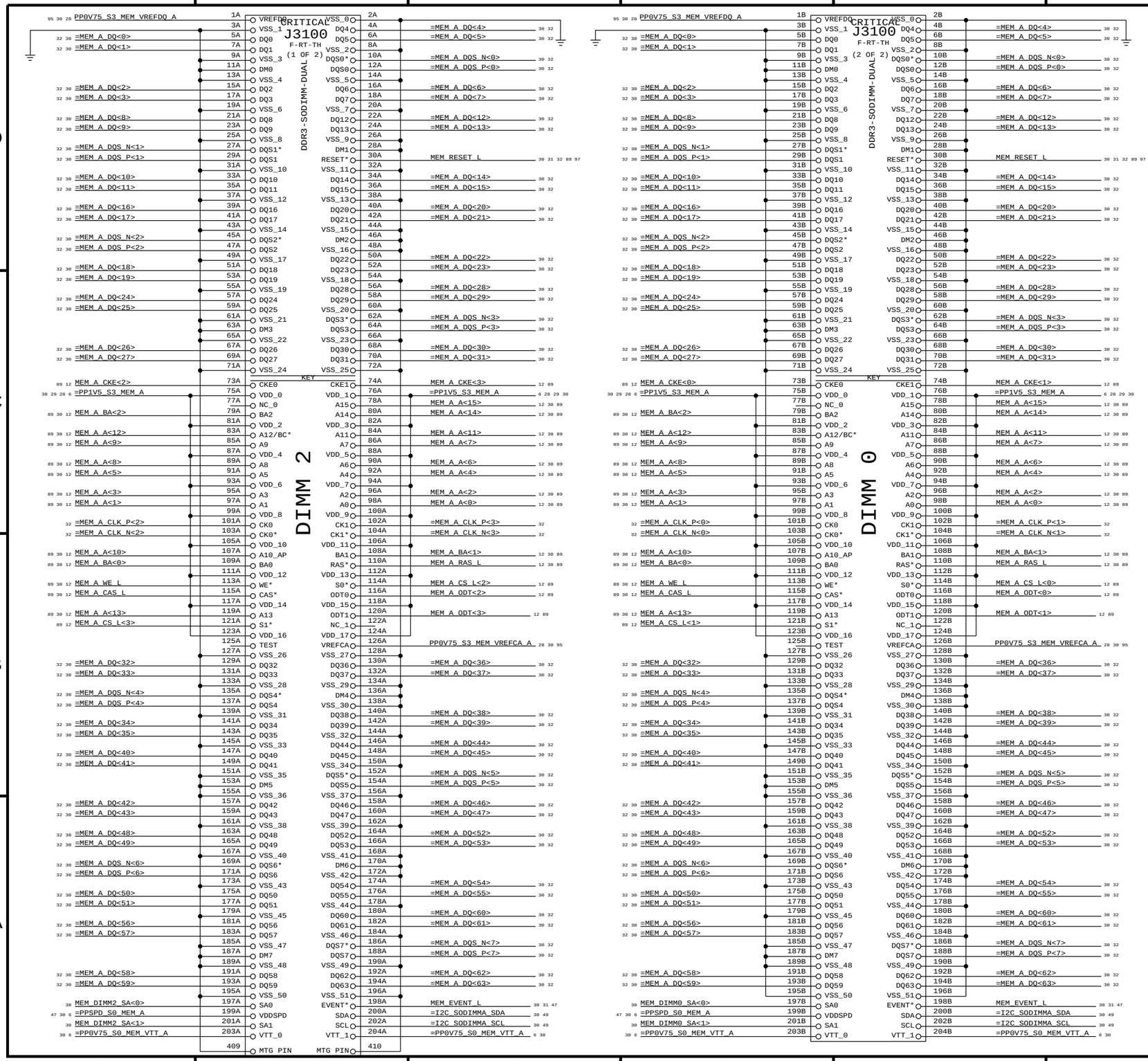

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SO-DIMM 0 & 2

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
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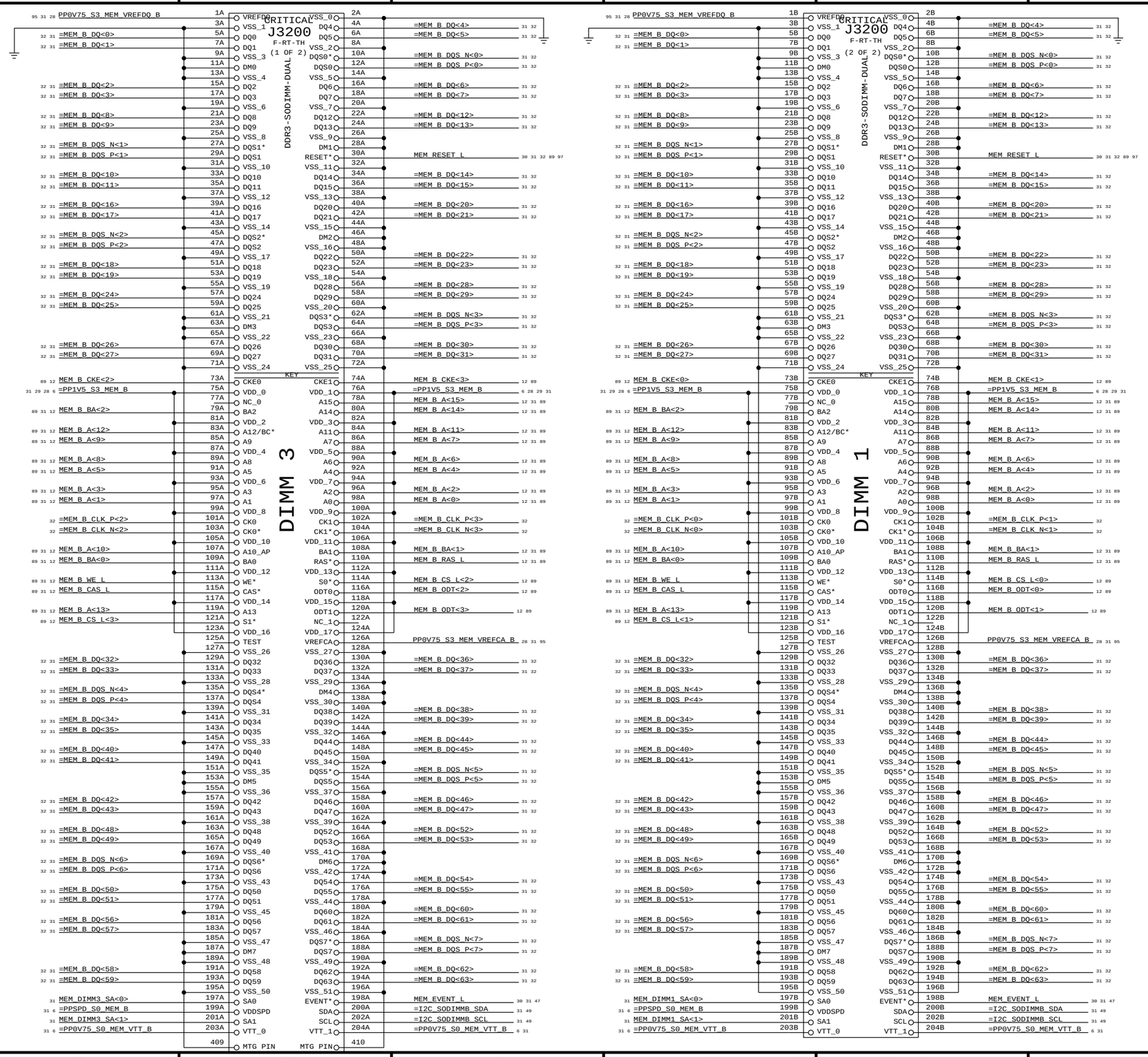

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SO-DIMM 1 & 3

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
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PAGE: 32 OF 110
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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<7>
MEM_A_DQS_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<7>

MEM_A_DQ<7> MAKE_BASE=TRUE =MEM_A_DQ<57>
MEM_A_DQ<6> MAKE_BASE=TRUE =MEM_A_DQ<56>
MEM_A_DQ<5> MAKE_BASE=TRUE =MEM_A_DQ<58>
MEM_A_DQ<4> MAKE_BASE=TRUE =MEM_A_DQ<59>
MEM_A_DQ<3> MAKE_BASE=TRUE =MEM_A_DQ<60>
MEM_A_DQ<2> MAKE_BASE=TRUE =MEM_A_DQ<61>
MEM_A_DQ<1> MAKE_BASE=TRUE =MEM_A_DQ<62>
MEM_A_DQ<0> MAKE_BASE=TRUE =MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<6>
MEM_A_DQS_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<6>

MEM_A_DQ<15> MAKE_BASE=TRUE =MEM_A_DQ<49>
MEM_A_DQ<14> MAKE_BASE=TRUE =MEM_A_DQ<52>
MEM_A_DQ<13> MAKE_BASE=TRUE =MEM_A_DQ<51>
MEM_A_DQ<12> MAKE_BASE=TRUE =MEM_A_DQ<50>
MEM_A_DQ<11> MAKE_BASE=TRUE =MEM_A_DQ<48>
MEM_A_DQ<10> MAKE_BASE=TRUE =MEM_A_DQ<53>
MEM_A_DQ<9> MAKE_BASE=TRUE =MEM_A_DQ<55>
MEM_A_DQ<8> MAKE_BASE=TRUE =MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<5>
MEM_A_DQS_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<5>

MEM_A_DQ<23> MAKE_BASE=TRUE =MEM_A_DQ<40>
MEM_A_DQ<22> MAKE_BASE=TRUE =MEM_A_DQ<45>
MEM_A_DQ<21> MAKE_BASE=TRUE =MEM_A_DQ<46>
MEM_A_DQ<20> MAKE_BASE=TRUE =MEM_A_DQ<47>
MEM_A_DQ<19> MAKE_BASE=TRUE =MEM_A_DQ<41>
MEM_A_DQ<18> MAKE_BASE=TRUE =MEM_A_DQ<44>
MEM_A_DQ<17> MAKE_BASE=TRUE =MEM_A_DQ<43>
MEM_A_DQ<16> MAKE_BASE=TRUE =MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<4>
MEM_A_DQS_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<4>

MEM_A_DQ<31> MAKE_BASE=TRUE =MEM_A_DQ<37>
MEM_A_DQ<30> MAKE_BASE=TRUE =MEM_A_DQ<33>
MEM_A_DQ<29> MAKE_BASE=TRUE =MEM_A_DQ<35>
MEM_A_DQ<28> MAKE_BASE=TRUE =MEM_A_DQ<34>
MEM_A_DQ<27> MAKE_BASE=TRUE =MEM_A_DQ<36>
MEM_A_DQ<26> MAKE_BASE=TRUE =MEM_A_DQ<32>
MEM_A_DQ<25> MAKE_BASE=TRUE =MEM_A_DQ<38>
MEM_A_DQ<24> MAKE_BASE=TRUE =MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<3>
MEM_A_DQS_P<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<3>

MEM_A_DQ<39> MAKE_BASE=TRUE =MEM_A_DQ<28>
MEM_A_DQ<38> MAKE_BASE=TRUE =MEM_A_DQ<29>
MEM_A_DQ<37> MAKE_BASE=TRUE =MEM_A_DQ<27>
MEM_A_DQ<36> MAKE_BASE=TRUE =MEM_A_DQ<31>
MEM_A_DQ<35> MAKE_BASE=TRUE =MEM_A_DQ<25>
MEM_A_DQ<34> MAKE_BASE=TRUE =MEM_A_DQ<24>
MEM_A_DQ<33> MAKE_BASE=TRUE =MEM_A_DQ<26>
MEM_A_DQ<32> MAKE_BASE=TRUE =MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<2>
MEM_A_DQS_P<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<2>

MEM_A_DQ<47> MAKE_BASE=TRUE =MEM_A_DQ<17>
MEM_A_DQ<46> MAKE_BASE=TRUE =MEM_A_DQ<16>
MEM_A_DQ<45> MAKE_BASE=TRUE =MEM_A_DQ<22>
MEM_A_DQ<44> MAKE_BASE=TRUE =MEM_A_DQ<23>
MEM_A_DQ<43> MAKE_BASE=TRUE =MEM_A_DQ<21>
MEM_A_DQ<42> MAKE_BASE=TRUE =MEM_A_DQ<20>
MEM_A_DQ<41> MAKE_BASE=TRUE =MEM_A_DQ<18>
MEM_A_DQ<40> MAKE_BASE=TRUE =MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<1>
MEM_A_DQS_P<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<1>

MEM_A_DQ<55> MAKE_BASE=TRUE =MEM_A_DQ<12>
MEM_A_DQ<54> MAKE_BASE=TRUE =MEM_A_DQ<13>
MEM_A_DQ<53> MAKE_BASE=TRUE =MEM_A_DQ<10>
MEM_A_DQ<52> MAKE_BASE=TRUE =MEM_A_DQ<15>
MEM_A_DQ<51> MAKE_BASE=TRUE =MEM_A_DQ<8>
MEM_A_DQ<50> MAKE_BASE=TRUE =MEM_A_DQ<9>
MEM_A_DQ<49> MAKE_BASE=TRUE =MEM_A_DQ<11>
MEM_A_DQ<48> MAKE_BASE=TRUE =MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<0>
MEM_A_DQS_P<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<0>

MEM_A_DQ<63> MAKE_BASE=TRUE =MEM_A_DQ<5>
MEM_A_DQ<62> MAKE_BASE=TRUE =MEM_A_DQ<4>
MEM_A_DQ<61> MAKE_BASE=TRUE =MEM_A_DQ<3>
MEM_A_DQ<60> MAKE_BASE=TRUE =MEM_A_DQ<2>
MEM_A_DQ<59> MAKE_BASE=TRUE =MEM_A_DQ<1>
MEM_A_DQ<58> MAKE_BASE=TRUE =MEM_A_DQ<0>
MEM_A_DQ<57> MAKE_BASE=TRUE =MEM_A_DQ<7>
MEM_A_DQ<56> MAKE_BASE=TRUE =MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<7>
MEM_B_DQS_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<7>

MEM_B_DQ<7> MAKE_BASE=TRUE =MEM_B_DQ<61>
MEM_B_DQ<6> MAKE_BASE=TRUE =MEM_B_DQ<60>
MEM_B_DQ<5> MAKE_BASE=TRUE =MEM_B_DQ<62>
MEM_B_DQ<4> MAKE_BASE=TRUE =MEM_B_DQ<63>
MEM_B_DQ<3> MAKE_BASE=TRUE =MEM_B_DQ<56>
MEM_B_DQ<2> MAKE_BASE=TRUE =MEM_B_DQ<57>
MEM_B_DQ<1> MAKE_BASE=TRUE =MEM_B_DQ<58>
MEM_B_DQ<0> MAKE_BASE=TRUE =MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<6>
MEM_B_DQS_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<6>

MEM_B_DQ<15> MAKE_BASE=TRUE =MEM_B_DQ<51>
MEM_B_DQ<14> MAKE_BASE=TRUE =MEM_B_DQ<54>
MEM_B_DQ<13> MAKE_BASE=TRUE =MEM_B_DQ<53>
MEM_B_DQ<12> MAKE_BASE=TRUE =MEM_B_DQ<52>
MEM_B_DQ<11> MAKE_BASE=TRUE =MEM_B_DQ<48>
MEM_B_DQ<10> MAKE_BASE=TRUE =MEM_B_DQ<49>
MEM_B_DQ<9> MAKE_BASE=TRUE =MEM_B_DQ<50>
MEM_B_DQ<8> MAKE_BASE=TRUE =MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<5>
MEM_B_DQS_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<5>

MEM_B_DQ<23> MAKE_BASE=TRUE =MEM_B_DQ<45>
MEM_B_DQ<22> MAKE_BASE=TRUE =MEM_B_DQ<40>
MEM_B_DQ<21> MAKE_BASE=TRUE =MEM_B_DQ<42>
MEM_B_DQ<20> MAKE_BASE=TRUE =MEM_B_DQ<47>
MEM_B_DQ<19> MAKE_BASE=TRUE =MEM_B_DQ<44>
MEM_B_DQ<18> MAKE_BASE=TRUE =MEM_B_DQ<41>
MEM_B_DQ<17> MAKE_BASE=TRUE =MEM_B_DQ<46>
MEM_B_DQ<16> MAKE_BASE=TRUE =MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<4>
MEM_B_DQS_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<4>

MEM_B_DQ<31> MAKE_BASE=TRUE =MEM_B_DQ<32>
MEM_B_DQ<30> MAKE_BASE=TRUE =MEM_B_DQ<39>
MEM_B_DQ<29> MAKE_BASE=TRUE =MEM_B_DQ<37>
MEM_B_DQ<28> MAKE_BASE=TRUE =MEM_B_DQ<38>
MEM_B_DQ<27> MAKE_BASE=TRUE =MEM_B_DQ<35>
MEM_B_DQ<26> MAKE_BASE=TRUE =MEM_B_DQ<34>
MEM_B_DQ<25> MAKE_BASE=TRUE =MEM_B_DQ<36>
MEM_B_DQ<24> MAKE_BASE=TRUE =MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<3>
MEM_B_DQS_P<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<3>

MEM_B_DQ<39> MAKE_BASE=TRUE =MEM_B_DQ<28>
MEM_B_DQ<38> MAKE_BASE=TRUE =MEM_B_DQ<24>
MEM_B_DQ<37> MAKE_BASE=TRUE =MEM_B_DQ<31>
MEM_B_DQ<36> MAKE_BASE=TRUE =MEM_B_DQ<30>
MEM_B_DQ<35> MAKE_BASE=TRUE =MEM_B_DQ<29>
MEM_B_DQ<34> MAKE_BASE=TRUE =MEM_B_DQ<25>
MEM_B_DQ<33> MAKE_BASE=TRUE =MEM_B_DQ<27>
MEM_B_DQ<32> MAKE_BASE=TRUE =MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<2>
MEM_B_DQS_P<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<2>

MEM_B_DQ<47> MAKE_BASE=TRUE =MEM_B_DQ<18>
MEM_B_DQ<46> MAKE_BASE=TRUE =MEM_B_DQ<20>
MEM_B_DQ<45> MAKE_BASE=TRUE =MEM_B_DQ<23>
MEM_B_DQ<44> MAKE_BASE=TRUE =MEM_B_DQ<22>
MEM_B_DQ<43> MAKE_BASE=TRUE =MEM_B_DQ<19>
MEM_B_DQ<42> MAKE_BASE=TRUE =MEM_B_DQ<21>
MEM_B_DQ<41> MAKE_BASE=TRUE =MEM_B_DQ<17>
MEM_B_DQ<40> MAKE_BASE=TRUE =MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<1>
MEM_B_DQS_P<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<1>

MEM_B_DQ<55> MAKE_BASE=TRUE =MEM_B_DQ<8>
MEM_B_DQ<54> MAKE_BASE=TRUE =MEM_B_DQ<14>
MEM_B_DQ<53> MAKE_BASE=TRUE =MEM_B_DQ<10>
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MEM_B_DQ<51> MAKE_BASE=TRUE =MEM_B_DQ<9>
MEM_B_DQ<50> MAKE_BASE=TRUE =MEM_B_DQ<15>
MEM_B_DQ<49> MAKE_BASE=TRUE =MEM_B_DQ<12>
MEM_B_DQ<48> MAKE_BASE=TRUE =MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<0>
MEM_B_DQS_P<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<0>

MEM_B_DQ<63> MAKE_BASE=TRUE =MEM_B_DQ<2>
MEM_B_DQ<62> MAKE_BASE=TRUE =MEM_B_DQ<1>
MEM_B_DQ<61> MAKE_BASE=TRUE =MEM_B_DQ<3>
MEM_B_DQ<60> MAKE_BASE=TRUE =MEM_B_DQ<7>
MEM_B_DQ<59> MAKE_BASE=TRUE =MEM_B_DQ<4>
MEM_B_DQ<58> MAKE_BASE=TRUE =MEM_B_DQ<5>
MEM_B_DQ<57> MAKE_BASE=TRUE =MEM_B_DQ<6>
MEM_B_DQ<56> MAKE_BASE=TRUE =MEM_B_DQ<0>

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	L	H
H	L	X	X	H	L
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

=PP3V3_S3_MEMRESET
R3350 20K 5% 1/16W MF-LF 402
=PP5V_S3_MEMRESET
R3351 20K 5% 1/16W MF-LF 402
R3352 20K 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM
ISOLATE_CPU_MEM_L_R1
Q3306 2N7002DW-X-G SOT-363
Q3306 2N7002DW-X-G SOT-363
CPU_MEM_RESET_L
=PP1V5_S3_MEMRESET
NOSTUFF R3355 0 5% 1/16W MF-LF 402
C3353 0.0022UF 20% 16V CERM 402
R3353 20K 5% 1/16W MF-LF 402
Q3304 2N7002 SOT23-HF1
MEM_RESET_L
ISOLATE_CPU_MEM_5V_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW C3300 0.1UF 20% 16V CERM 402
U3300 74LVC74ABQ DHVQFN
MEM_RESET_HW
PM_SLP_S4_L
PM_SYS_PWRGD
=PP3V3_S3_MEMRESET
PM_SLP_S4_D_L
=PP3V3_S3_MEMRESET
CPU_MEM_RESET3V3_L
PM_SLP_S3_L
THRM GND_PAD
PM_SLP_S4_D_L
TP_PM_SLP_S4_D
ISOLATE_CPU_MEMHW_L
TP_ISOLATE_CPU
R3385 0 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM_L
NOSTUFF R3383 0 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM_L_R1
MEM_RESET_HW R3380 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET_L
CPU_MEM_RESET_R_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW R3381 10K 5% 1/16W MF-LF 402
MEM_RESET_HW R3382 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET3V3
CPU_MEM_RESET3V3_L
MEM_RESET_HW
Q3360 2N3904 SOT23-HF
MEM_RESET_HW Q3350 2N7002 SOT23-HF1

NOSTUFF R3390 0 5% 1/16W MF-LF 402
ALL_SYS_PWRGD_R
=PP3V3_S5_MEMRESET
NOSTUFF C3390 0.1UF 20% 16V CERM 402
NOSTUFF R3391 0 5% 1/16W MF-LF 402
PM_EN_DDRVTT_S0_REG
DDRSYS_EN
NOSTUFF MC74VHC1G08 SOT23-5-HF
U3390
NOSTUFF R3393 0 5% 1/16W MF-LF 402
SLP_S3_CTL_L
R3394 0 5% 1/16W MF-LF 402
PM_SLP_S3_L
PM_SLP_S3_5V_R2

=PP5V_S3_MEMRESET
R3387 20K 5% 1/16W MF-LF 402
R3384 20K 5% 1/16W MF-LF 402
PM_SLP_S3_5V
PM_SLP_S3_5V_L
Q3370 2N7002DW-X-G SOT-363
Q3370 2N7002DW-X-G SOT-363

NOSTUFF R3386 0 5% 1/16W MF-LF 402
Q3375 FDMC8296 POWER33
=PP0V75_S0_MEM_VTT_S0FET
PPVTT_S0_DDR_FET
R3340 100K 5% 1/16W MF-LF 402
PM_SLP_S3_5V_L
R3388 10 5% 1/16W MF-LF 402
VTT_R
PM_SLP_S3_5V
Q3380 2N7002 SOT23-HF1

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<0>
MEM_A_CLK_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<0>
MEM_A_CLK_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<1>
MEM_A_CLK_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<1>
MEM_A_CLK_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<2>
MEM_A_CLK_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<2>
MEM_A_CLK_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<3>
MEM_A_CLK_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<3>

MEM_B_CLK_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<0>
MEM_B_CLK_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<0>
MEM_B_CLK_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<1>
MEM_B_CLK_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<1>
MEM_B_CLK_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<2>
MEM_B_CLK_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<2>
MEM_B_CLK_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<3>
MEM_B_CLK_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<3>

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
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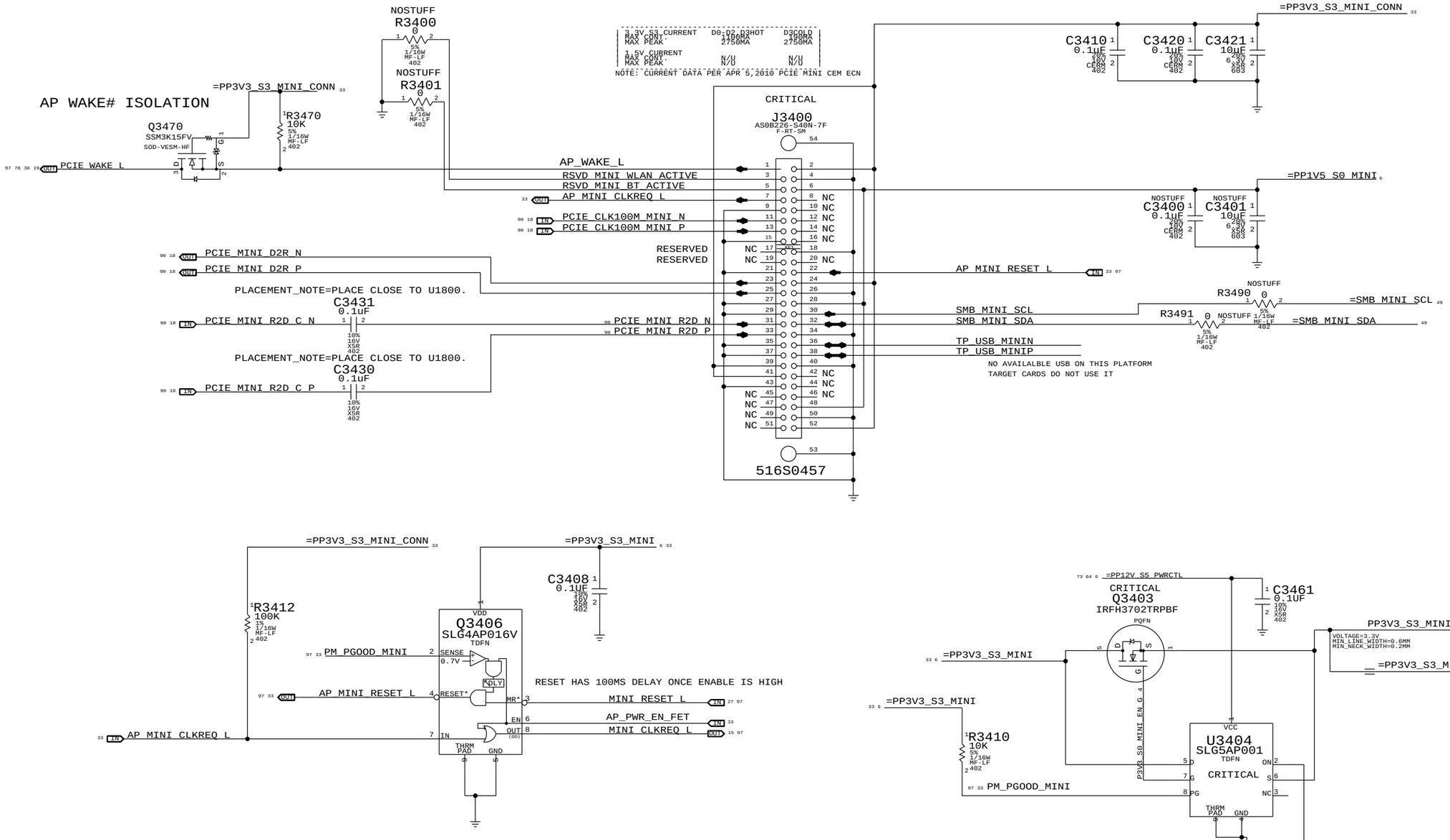

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

PCI-E Wireless Connector

Apple Inc.

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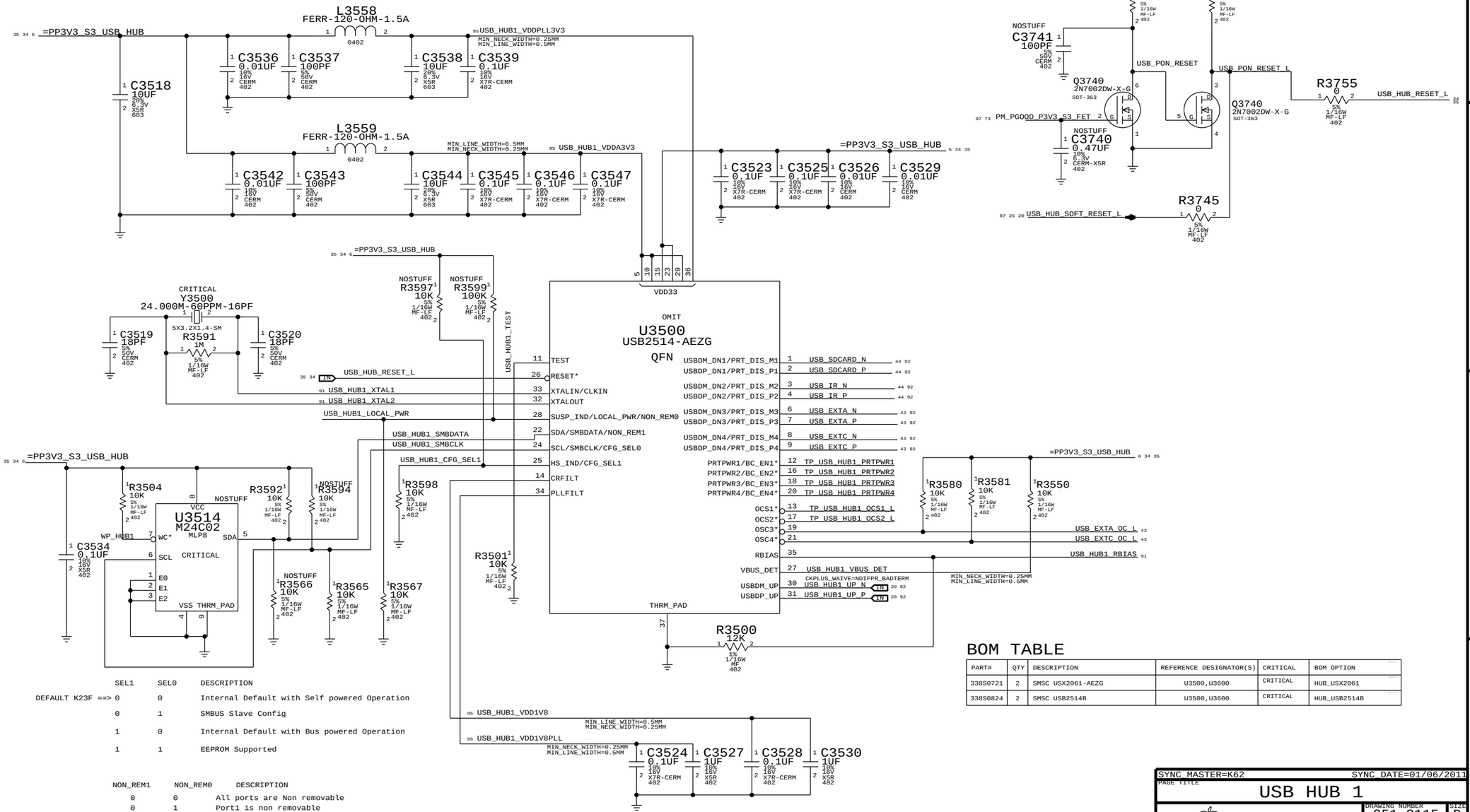
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

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USB HUB-2

L3658 FERR-120-OHM-1.5A 0402
=PP3V3_S3_USB_HUB
95USB_HUB2_VDDPLL3V3
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C3636 0.01UF 10% 16V CERM 402
C3637 100PF 5% 50V CERM 402
C3638 10UF 20% 6.3V X5R 603
C3639 0.1UF 10% 16V X7R-CERM 402
C3618 10UF 20% 6.3V X5R 603

L3629 FERR-120-OHM-1.5A 0402
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
95USB_HUB2_VDDA3V3
C3642 0.01UF 10% 16V CERM 402
C3643 100PF 5% 50V CERM 402
C3644 10UF 20% 6.3V X5R 603
C3645 0.1UF 10% 16V X7R-CERM 402
C3646 0.1UF 10% 16V X7R-CERM 402
C3647 0.1UF 10% 16V X7R-CERM 402

=PP3V3_S3_USB_HUB
C3623 0.1UF 10% 16V X7R-CERM 402
C3625 0.1UF 10% 16V X7R-CERM 402
C3626 0.01UF 10% 16V CERM 402
C3629 0.01UF 10% 16V CERM 402

=PP3V3_S3_USB_HUB
CRITICAL
Y3600 24.000M-60PPM-16PF 5X3.2X1.4-SM
C3619 18PF 5% 50V CERM 402
R3691 1M 5% 1/10W MF-LF 402
C3620 18PF 5% 50V CERM 402
NOSTUFF R3697 10K 5% 1/10W MF-LF 402
NOSTUFF R3699 100K 5% 1/10W MF-LF 402

VDD33
OMIT
U3600 USB2514-AEZG QFN

USB_HUB2_TEST 11 TEST
34 USB_HUB_RESET_L 26 RESET*
91 USB_HUB2_XTAL1 33 XTALIN/CLKIN
91 USB_HUB2_XTAL2 32 XTALOUT
USB_HUB2_LOCAL_PWR 28 SUSP_IND/LOCAL_PWR/NON_REM0
USB_HUB2_SMBDATA 22 SDA/SMBDATA/NON_REM1
USB_HUB2_SMBCLK 24 SCL/SMBCLK/CFG_SEL0
USB_HUB2_CFG_SEL1 25 HS_IND/CFG_SEL1
14 CRFILT
34 PLLFILT

USBDM_DN1/PRT_DIS_M1 1 USB_BT_N 44 92
USBDP_DN1/PRT_DIS_P1 2 USB_BT_P 44 92
USBDM_DN2/PRT_DIS_M2 3 USB_HUB2UNUSED_N 92
USBDP_DN2/PRT_DIS_P2 4 USB_HUB2UNUSED_P 92
USBDM_DN3/PRT_DIS_M3 6 USB_EXTB_N 43 92
USBDP_DN3/PRT_DIS_P3 7 USB_EXTB_P 43 92
USBDM_DN4/PRT_DIS_M4 8 USB_EXTD_N 43 92
USBDP_DN4/PRT_DIS_P4 9 USB_EXTD_P 43 92
PRTPWR1/BC_EN1* 12 TP_USB_HUB2_PRTPWR1
PRTPWR2/BC_EN2* 16 TP_USB_HUB2_PRTPWR2
PRTPWR3/BC_EN3* 18 TP_USB_HUB2_PRTPWR3
PRTPWR4/BC_EN4* 20 TP_USB_HUB2_PRTPWR4
OCS1* 13 TP_USB_HUB2_OCS1
OCS2* 17 TP_USB_HUB2_OCS2
OSC3* 19 USB_EXTB_OC_L 43
OSC4* 21 USB_EXTD_OC_L 43
RBIAS 35 USB_HUB2_RBIAS 91
VBUS_DET 27 USB_HUB2_VBUS_DET
USBDM_UP 30 CKPLUS_WAIVE=NDIFPR_BADTERM USB_HUB2_UP_N 20 92
USBDP_UP 31 USB_HUB2_UP_P 20 92
THRM_PAD 37

=PP3V3_S3_USB_HUB
R3660 10K 5% 1/10W MF-LF 402
R3661 10K 5% 1/10W MF-LF 402

=PP3V3_S3_USB_HUB
R3604 10K 5% 1/10W MF-LF 402
NOSTUFF
U3614 M24C02 MLP8 CRITICAL
VCC SDA SCL WP_HUB2 WC* E0 E1 E2 VSS THRM_PAD
C3634 0.1UF 10% 16V X5R 402
R3692 10K 5% 1/10W MF-LF 402
NOSTUFF R3694 10K 5% 1/10W MF-LF 402
R3698 10K 5% 1/10W MF-LF 402
R3601 10K 5% 1/10W MF-LF 402
NOSTUFF R3665 10K 5% 1/10W MF-LF 402
R3666 10K 5% 1/10W MF-LF 402
R3667 10K 5% 1/10W MF-LF 402

=PP3V3_S3_USB_HUB
R3680 10K 5% 1/10W MF-LF 402
R3681 10K 5% 1/10W MF-LF 402
R3682 10K 5% 1/10W MF-LF 402

R3600 12K 1% 1/10W MF 402

95USB_HUB2_VDD1V8
95USB_HUB2_VDD1V8PLL
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.5MM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C3624 0.1UF 10% 16V X7R-CERM 402
C3627 1UF 10% 16V X5R 402
C3628 0.1UF 10% 16V X7R-CERM 402
C3630 1UF 10% 16V X5R 402

SYNC_MASTER=K62 SYNC_DATE=01/06/2011
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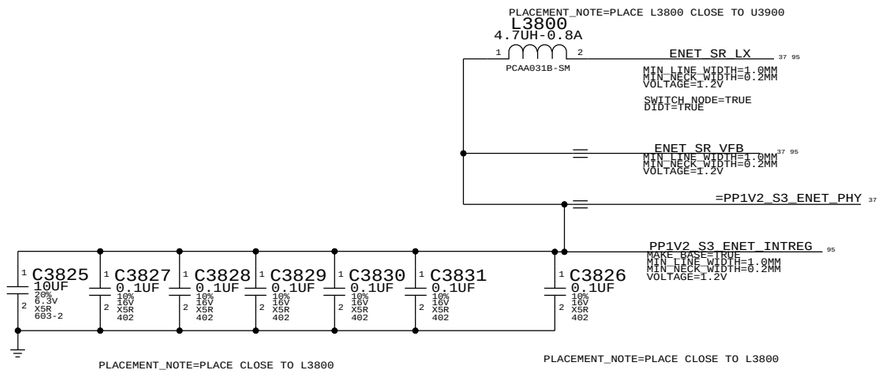
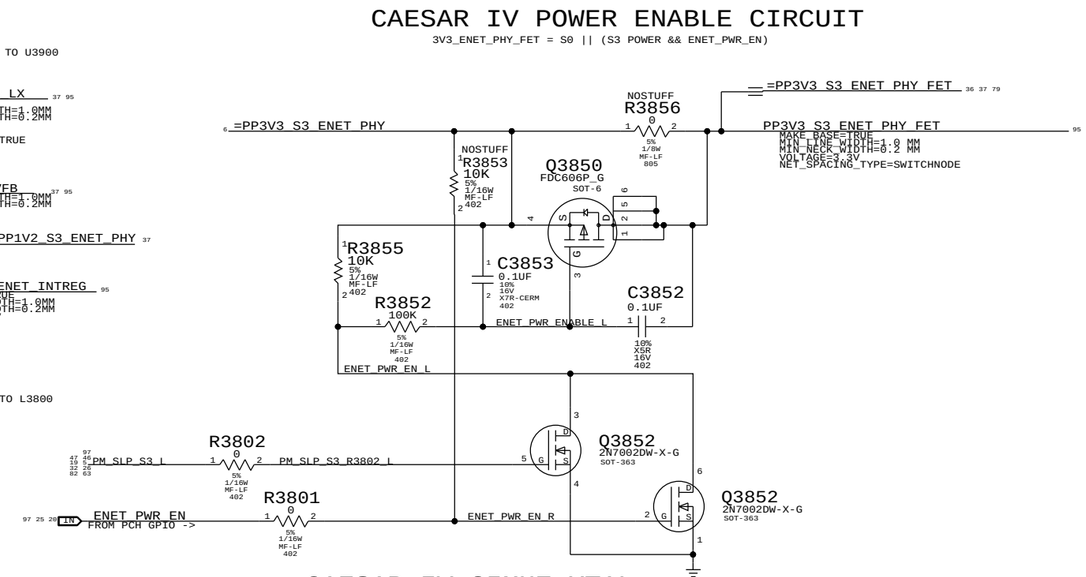
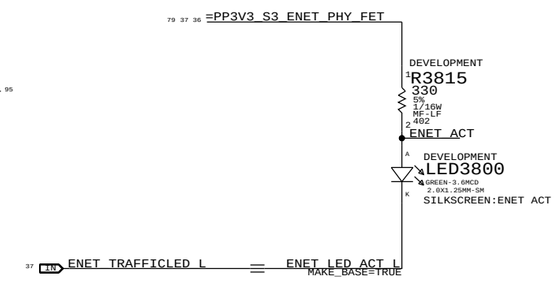
CAESAR IV 1.2V INT.VR CMPTS



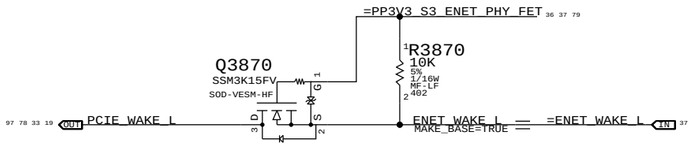
CAESAR IV POWER ENABLE CIRCUIT



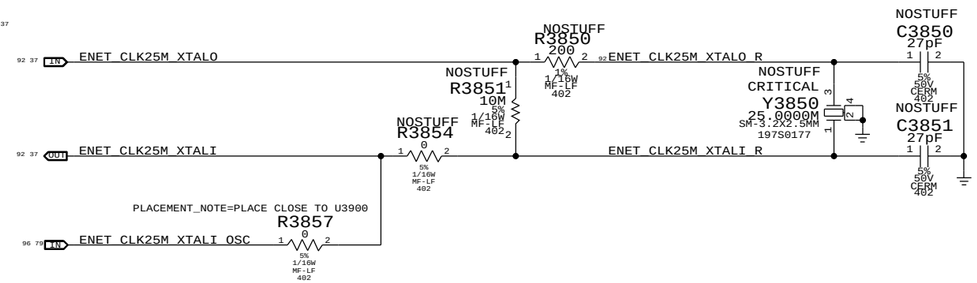
CAESAR IV ACTIVITY LED



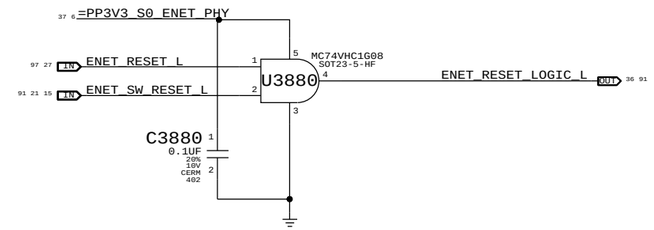
CAESAR IV WAKE# ISOLATION



CAESAR IV 25MHZ XTAL

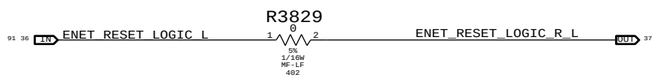


CAESAR IV SW RESET GATING

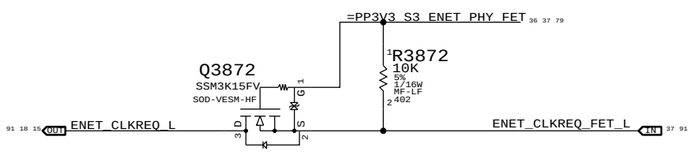


CAESAR IV STRAPS (NONE)

CAESAR IV RESET CONNECTION



CAESAR IV CLKREQ ISOLATION



CAESAR IV SUPPORT

Apple Inc.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

79 37 36 =PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF-LF 402 — 95 ENET_3V3_S3_SR_IN
SWITCH_NODE=TRUE
DIDT=TRUE
NET_SPACING_TYPE=SWITCHNODE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3980 0.1UF 10% 16V X5R 402
C3981 0.1UF 10% 16V X5R 402
C3979 4.7UF 20% 6.3V CERM 603

VDD for Card Reader I/O
37 =PP3V3R1V8_ENET_LR_OUT

CRITICAL
L3900 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3900 0 5% 1/16W MF-LF 402 — 95 ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3905 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3910 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402

C3917 0.1UF 10% 16V X7R-CERM 402
C3918 0.1UF 10% 16V X7R-CERM 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

ENET_SR_LX 36 95
ENET_SR_VFB 36 95

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY 36
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3925 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3930 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

42 AVDDH
48
37 BIASVDDH
17 XTALVDDH
7
20 VDDO
56
62
14 SR_VDD
15 SR_VDDP
16 SR_LX
13 SR_VFB
39
45 AVDDL
51
29 PCIE_PLLVDDL
32 GPHY_PLLVDDL
36
35 VDDC
61

OMIT
U3900
BCM57765
QFN-8X8

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for
the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 37
PP3V3R1V8_ENET_LR_OUT_REG 95
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

DEVELOPMENT C3970 4.7UF 10% 6.3V X5R-CERM 603
DEVELOPMENT C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402
DEVELOPMENT
NOSTUFF R3959 150 5% 1/16W MF-LF 402
NOSTUFF C3959 10PF 5% 50V CERM 402

MUST DO: REMOVE C/R3959 AFTER PROTO 2

36 6 =PP3V3_S0_ENET_PHY

R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

92 18 OUT PCIE_ENET_D2R_N
92 18 OUT PCIE_ENET_D2R_P
92 18 IN PCIE_ENET_R2D_C_P
92 18 IN PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402
36 IN =ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD-ENET)
92 PCIE_ENET_D2R_C_N — 27 PCIE_TXD_N
92 PCIE_ENET_D2R_C_P — 28 PCIE_TXD_P
92 PCIE_ENET_R2D_P — 33 PCIE_RXD_P
92 PCIE_ENET_R2D_N — 34 PCIE_RXD_N
90 18 IN PCIE_CLK100M_ENET_P — 31 PCIE_REFCLK_P
90 18 IN PCIE_CLK100M_ENET_N — 30 PCIE_REFCLK_N
36 IN ENET_RESET_LOGIC_R_L — 11 PERST* (IPD)
91 36 OUT ENET_CLKREQ_FET_L — 12 CLKREQ* (OD)
ENET_WAKE_R_L — 3 WAKE* (OD)
97 21 15 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
ENET_SMB_CLK — 6 SMB_CLK
ENET_SMB_DATA — 10 SMD_DATA (IPD-ENETM)
37 BI ENET_SCLK — 66 SCLK
37 IN ENET_MISO — 64 SI/LINKLED*
37 BI ENET_MOSI — 65 SO
37 BI ENET_CS_L — 63 CS*
(IPU)
TP_ENET_SPD100LED_L — 2 SPD100LED*/SERIAL_DO (OD)
36 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
92 36 IN ENET_CLK25M_XTALI — 18 XTALI
92 36 OUT ENET_CLK25M_XTALO — 19 XTALO
92 ENET_RDAC — 38 RDAC

R3965 1.24K 1% 1/16W MF-LF 402

(NO IPU OR IPD-ENET) THRM_PAD 69

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

TRD0_P 40 — ENETCONN_MDI_P<0>
TRD0_N 41 — ENETCONN_MDI_N<0>
TRD1_P 44 — ENETCONN_MDI_P<1>
TRD1_N 43 — ENETCONN_MDI_N<1>
TRD2_P 46 — ENETCONN_MDI_P<2>
TRD2_N 47 — ENETCONN_MDI_N<2>
TRD3_P 50 — ENETCONN_MDI_P<3>
TRD3_N 49 — ENETCONN_MDI_N<3>
(all B4 38 92)

(IPD) GPIO_0 5 — NC
GPIO_1/CR_BUS_PWR 8
RE*/GPIO_2 9 — ENET_MEDIA_SENSE
(IPx-ENET) SD_DETECT/WE* 1 — 92 ENET_SD_DETECT_L
(IPU-ENET) CR_CMD/CLE 26 — 92 ENET_SD_CMD
CR_CLK/RY_BY* 21 — 92 ENET_SD_CLK
(IPU-ENET) CR_DATA0 25 — ENET_CR_DATA<0>
CR_DATA1 24 — ENET_CR_DATA<1>
CR_DATA2 23 — ENET_CR_DATA<2>
CR_DATA3 22 — ENET_CR_DATA<3>
CR_DATA4 52 — ENET_CR_DATA<4>
CR_DATA5 53 — ENET_CR_DATA<5>
CR_DATA6 54 — ENET_CR_DATA<6>
CR_DATA7 55 — ENET_CR_DATA<7>
(all 92)

(IPU-ENET) CE*/MS_INS* 59 — NC_ENET_CE_L_MS_INS_L NO_TEST=TRUE
(IPU-ENET) CR_LED/ALE 60 — ENET_CR_PWREN
(IPU-ENET) CR_WP*/XD_WP* 57
XD_DETECT 68 — ENET_SR_DISABLE

R3960 0 DEVELOPMENT — SDCONN_DETECT_L
R3961 33 DEVELOPMENT — SDCONN_CMD
R3979 33 DEVELOPMENT — SDCONN_CLK
PLACEMENT_NOTE=PLACE NEAR U3900
R3971 33 DEVELOPMENT — SDCONN_DATA<0>
R3972 33 DEVELOPMENT — SDCONN_DATA<1>
R3973 33 DEVELOPMENT — SDCONN_DATA<2>
R3974 33 DEVELOPMENT — SDCONN_DATA<3>
R3975 33 DEVELOPMENT — SDCONN_DATA<4>
R3976 33 DEVELOPMENT — SDCONN_DATA<5>
R3977 33 DEVELOPMENT — SDCONN_DATA<6>
R3978 33 DEVELOPMENT — SDCONN_DATA<7>
(all 5% 1/16W MF-LF 402; SDCONN_* B4 45 92)

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

SDCONN_WP IN 45
R3980 1K NOSTUFF — =PP3V3_S3_ENET_PHY_FET 36 37 79
R3981 1K

ENET supports both active-levels for WP.

(See note)
ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

79 37 36 =PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF-LF 402
R3992 4.7K 5% 1/16W MF-LF 402
R3904 0 5% 1/16W MF-LF 402

U3990
AT45DB021D
SOIC-8S1
OMIT_TABLE

C3990 0.1UF 10% 16V X7R-CERM 402

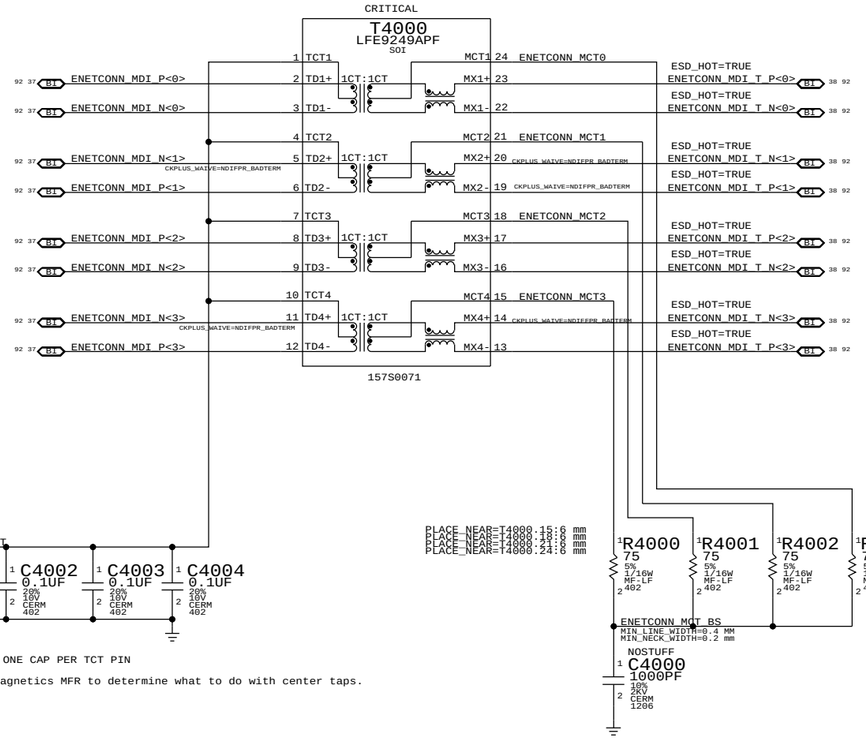
37 IN ENET_SCLK — ENET_SCLK_R — SCK
37 IN ENET_CS_L — CS*
ENET_SWP_L — WP*
ENET_SRESET_L — RESET*
SI — ENET_MOSI IN 37
SO — ENET_MISO OUT 37
VCC
GND

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

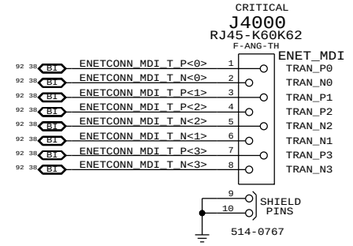
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K62 SYNC_DATE=01/06/2013
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 39 OF 110
SHEET 37 OF 98

THIS PAGE DIFFERENT BETWEEN K60 and K62.



NO PAIR AND PIN POLARITY SWAPS



SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE: Ethernet Connector

Apple Inc.

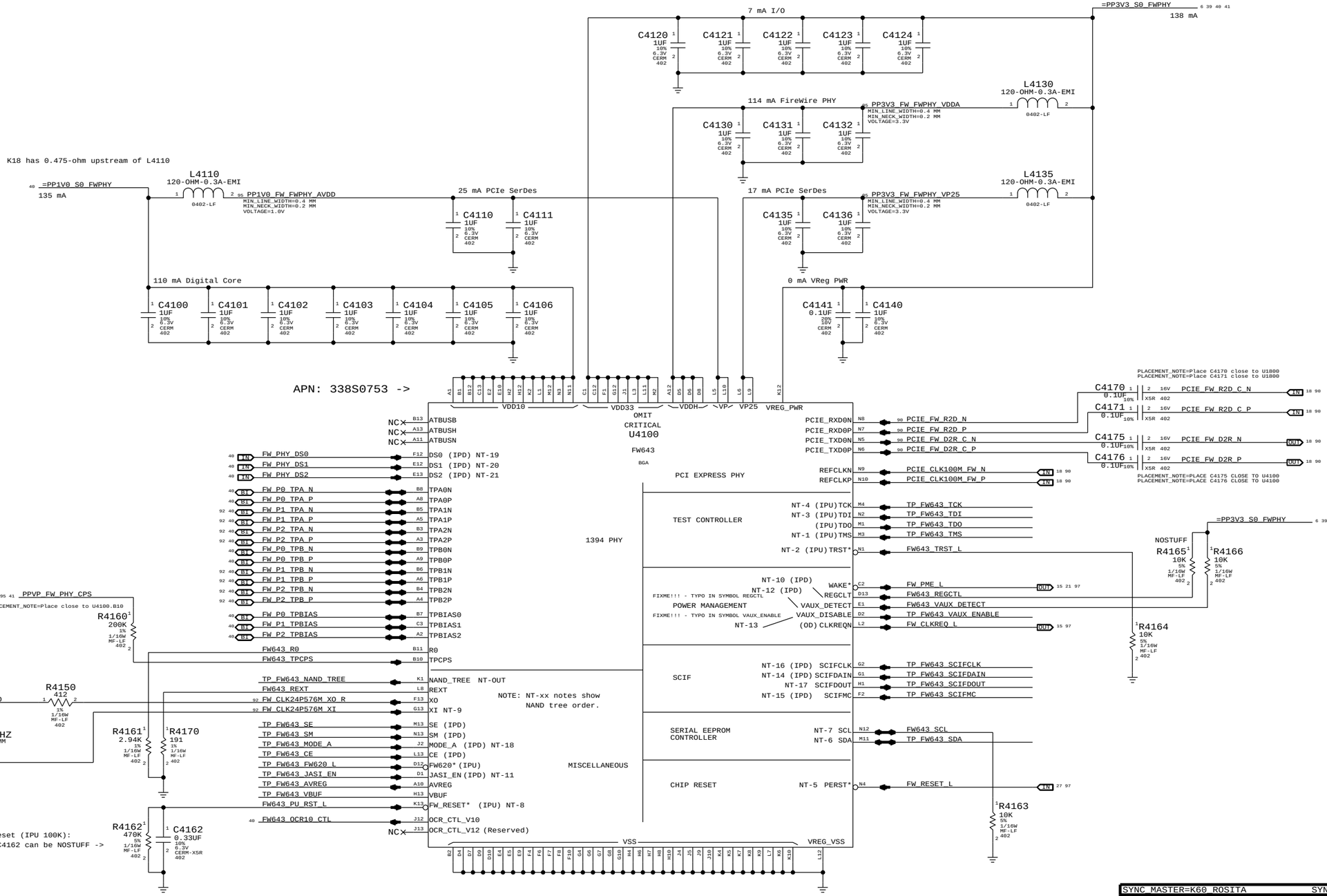
DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 40 OF 110

SHEET: 38 OF 98



SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
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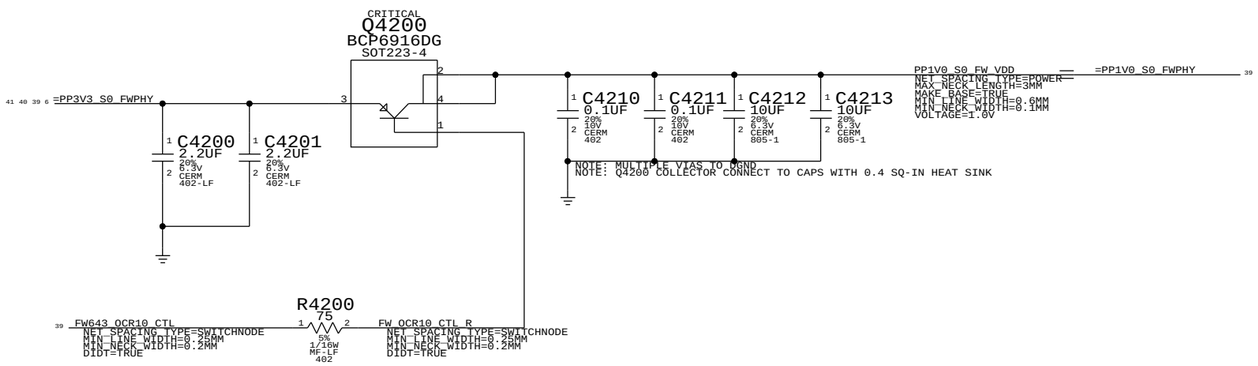
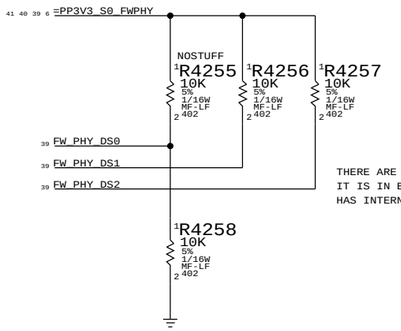
FW643 1.0V GENERATION



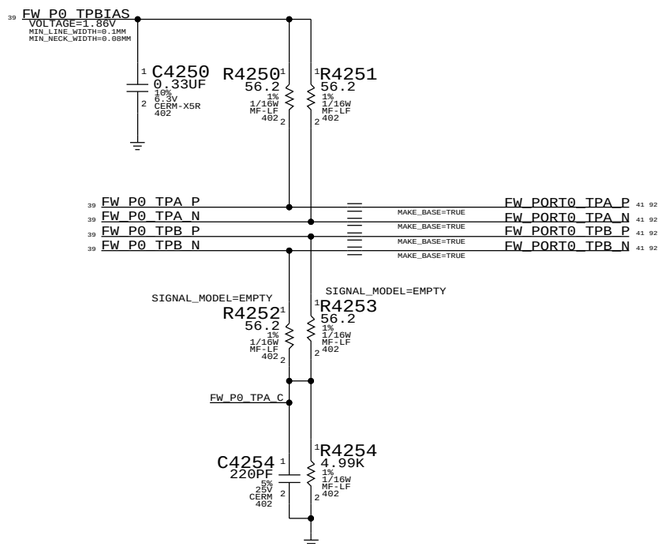
1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS		NC_FW_PORT1_TPBIAS
FW_P1_TPA_P		NC_FW_PORT1_TPA_P
FW_P1_TPA_N		NC_FW_PORT1_TPA_N
FW_P1_TPB_P		NC_FW_PORT1_TPB_P
FW_P1_TPB_N		NC_FW_PORT1_TPB_N
FW_P2_TPBIAS		NC_FW_PORT2_TPBIAS
FW_P2_TPA_P		NC_FW_PORT2_TPA_P
FW_P2_TPA_N		NC_FW_PORT2_TPA_N
FW_P2_TPB_P		NC_FW_PORT2_TPB_P
FW_P2_TPB_N		NC_FW_PORT2_TPB_N

MAKE_BASE=TRUE
NO_TEST=TRUE

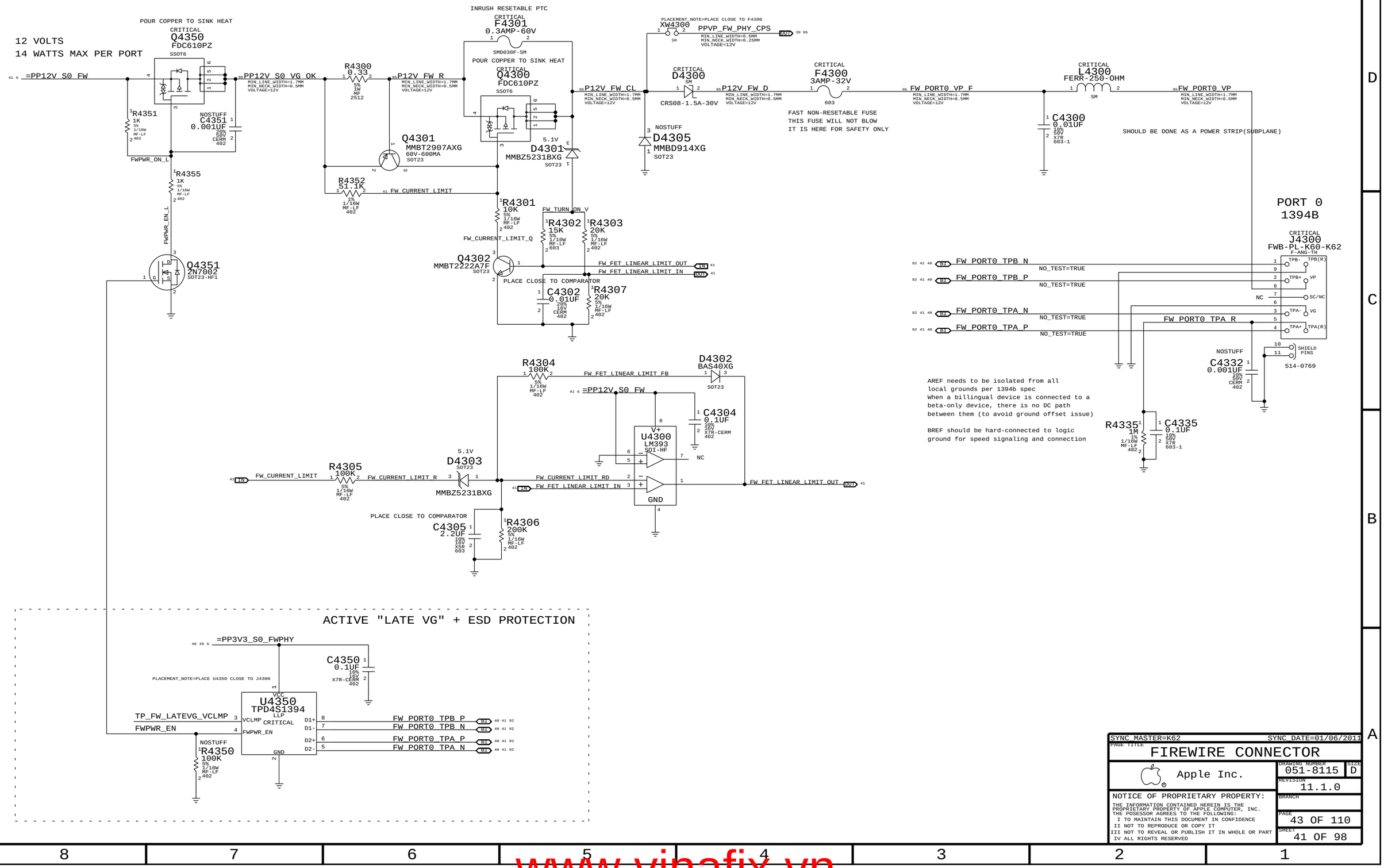
NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 42 OF 110
SHEET 40 OF 98



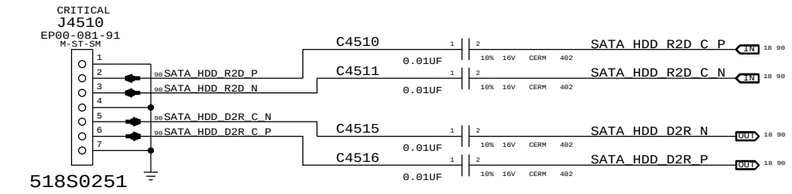
BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.
K60E should stuff S_P1_ODD:YES because it has no SSD option.

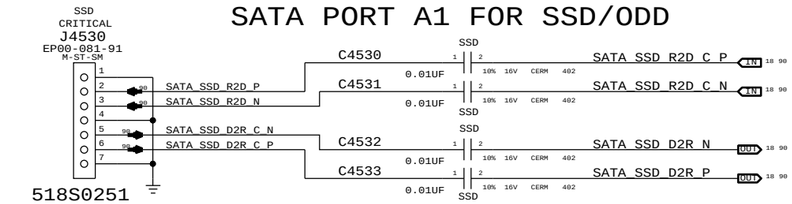
SILKSCREEN:SATA0

SATA PORT A0 FOR HDD



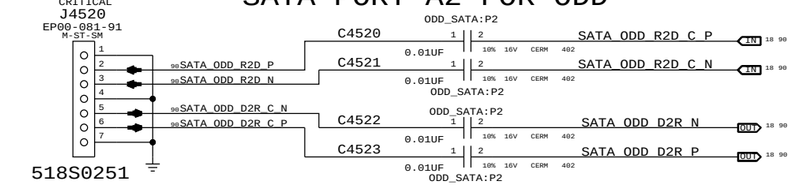
SILKSCREEN:SATA1

SATA PORT A1 FOR SSD/ODD

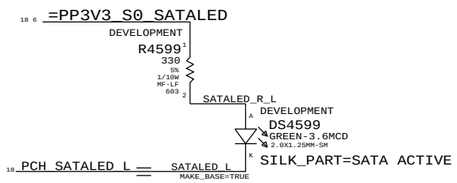


SILKSCREEN:SATA2
ODD_SATA:P2

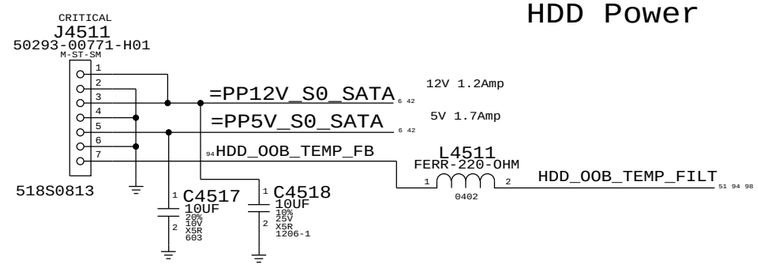
SATA PORT A2 FOR ODD



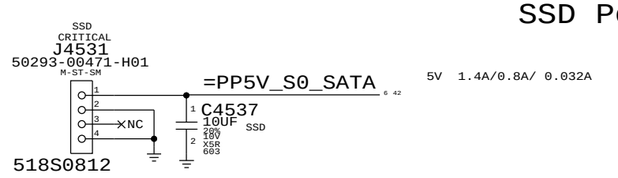
SATA Activity LED



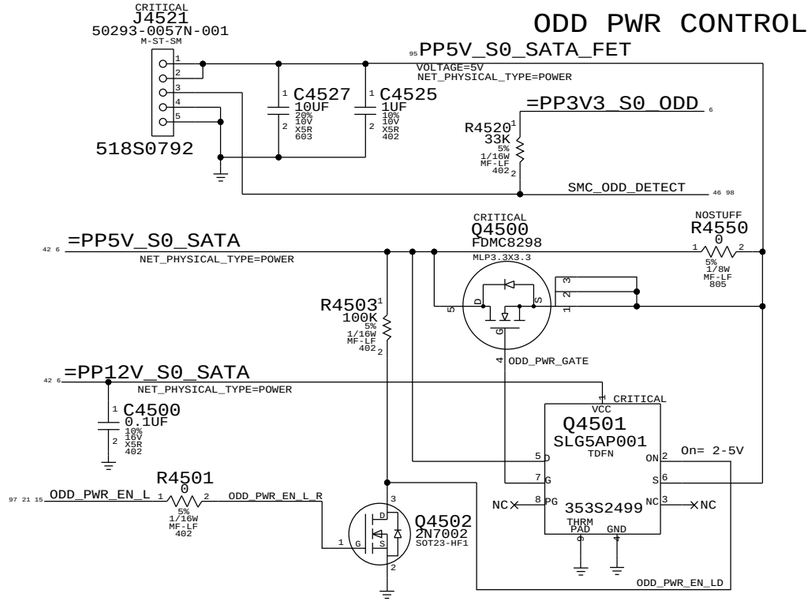
HDD Power



SSD Power



ODD PWR CONTROL



SYNC_MASTER=K60_JERRY	SYNC_DATE=01/06/2011
PAGE TITLE	SATA Connectors
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
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	BRANCH
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	SHEET 42 OF 98

USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL

Current Limit at 2.1Amp (@ S3 & S0)

=PP5V_S3_USB

U4600 TPS2561DR SON
IN_0, IN_1, OUT1, OUT2, FAULT1*, FAULT2*, ILIM, EN1, EN2, GND, THRM PAD

USB_EXTC_OC_L
USB_EXTD_OC_L

C4601 0.1UF 20% 10V CERM 402
C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL

R4600 23.2K 1% 1/16W MF-LF 402

Place R4600 very close to ILIM pin

PM_EN_USB_PWR

PP5V_USB_PORT3
155S0329 L4630 FERR-220-OHM-2.5A 0603 CRITICAL
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB_PORT2
155S0329 L4660 FERR-220-OHM-2.5A 0603 CRITICAL
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

C4603 0.1UF 20% 10V CERM 402
C4630 0.01uF 20% 16V CERM 402
C4661 0.1UF 20% 10V CERM 402
C4660 0.01uF 20% 16V CERM 402

(PUT CAP ON CONNECTOR SIDE)

=PP3V3_G3H_SMCUSBMUX
=PP3V3_S5_SMCUSBMUX
R4653 0 5% 1/10W MF-LF 402 NOSTUFF
R4654 0 5% 1/10W MF-LF 402 MOJOMUX:YES

PP3V3_SMCUSBMUX
C4650 0.1UF 20% 10V CERM 402 MOJOMUX:YES

PP5V_USB_PORT3_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

U4650 PI3USB102ZLE TQFN VCC
SMC_RX_L, SMC_TX_L, USB_EXTD_P, USB_EXTD_N
M+ MOJOMUX:YES, M- MOJOMUX:YES, Y+, Y-, D+, D-, OE*, SEL, GND

USB_D_MUXED_N, USB_D_MUXED_P

L4631 120-OHM-90MA DLP0NS CRITICAL

USB_PORT3_N, USB_PORT3_P

J4630 USB-K60K62 F-ANG-TH
VBUS, DATA-, DATA+, GND
514-0768

D4630 RCLAMP0502N SLP1210N6 CRITICAL
NC, IO, GND, VBUS

R4651 0 5% 1/10W MF-LF 402 MOJOMUX:NO
R4652 0 5% 1/10W MF-LF 402 MOJOMUX:NO

USB_DEBUGPRT_EN_L
SEL=1: CHOOSE USB
SEL=0: CHOOSE SMC

PP5V_USB_PORT2_F
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

PP5V_USB_PORT0
155S0329 L4600 FERR-220-OHM-2.5A 0603 CRITICAL
VOLTAGE=5V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM

PP5V_USB_PORT0_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

U4620 TPS2561DR SON
IN_0, IN_1, OUT1, OUT2, FAULT1*, FAULT2*, ILIM, EN1, EN2, GND, THRM PAD

=PP5V_S3_USB
USB_EXTA_OC_L
USB_EXTB_OC_L

C4621 0.1UF 20% 10V CERM 402
C4622 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL

R4620 23.2K 1% 1/16W MF-LF 402

Place R4620 very close to ILIM pin

PP5V_USB_PORT1
L4620 FERR-220-OHM-2.5A 0603 CRITICAL
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

C4633 0.1UF 20% 10V CERM 402
C4600 0.01uF 20% 16V CERM 402
C4623 0.1UF 20% 10V CERM 402
C4624 0.01uF 20% 16V CERM 402

(PUT CAP ON CONNECTOR SIDE)

PP5V_USB_PORT1_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

J4610 USB-MG6-K60-K62 F-ANG-TH
VBUS, DATA-, DATA+, GND
514-0770

L4611 120-OHM-90MA DLP0NS CRITICAL
USB_EXTB_N, USB_EXTB_P
USB_PORT1_N, USB_PORT1_P

D4610 RCLAMP0502N SLP1210N6 CRITICAL
NC, IO, GND, VBUS

L4621 120-OHM-90MA DLP0NS CRITICAL
USB_EXTC_N, USB_EXTC_P
USB_PORT2_N, USB_PORT2_P

J4620 USB-K60K62 F-ANG-TH
VBUS, DATA-, DATA+, GND
514-0768

D4620 RCLAMP0502N SLP1210N6 CRITICAL
NC, IO, GND, VBUS

L4601 120-OHM-90MA DLP0NS CRITICAL
USB_EXTA_N, USB_EXTA_P
USB_PORT0_N, USB_PORT0_P

J4600 USB-MG6-K60-K62 F-ANG-TH
VBUS, DATA-, DATA+, GND
514-0770

D4600 RCLAMP0502N SLP1210N6 CRITICAL
NC, IO, GND, VBUS

PORT 3

PORT 2

PORT 1

PORT 0

USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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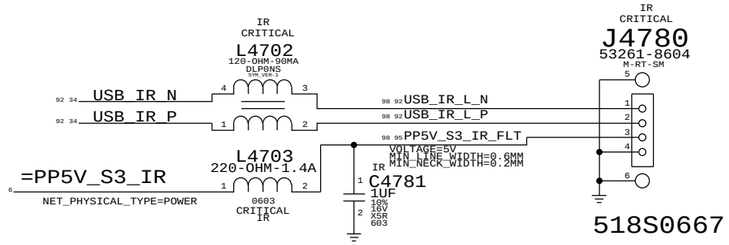
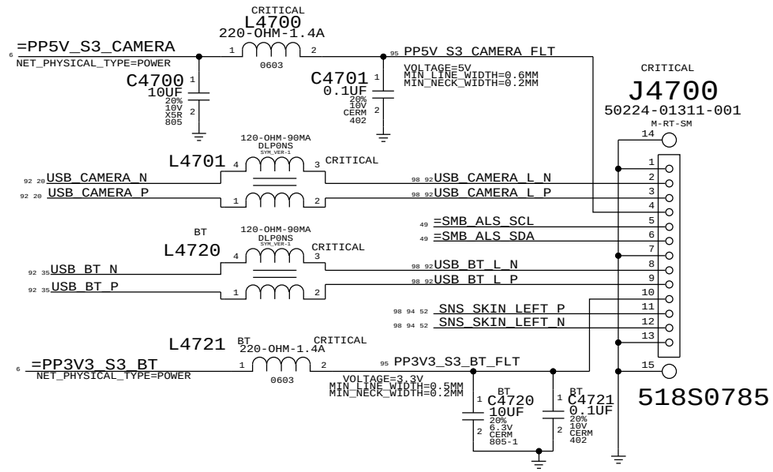
IR RECEIVER CONNECTOR

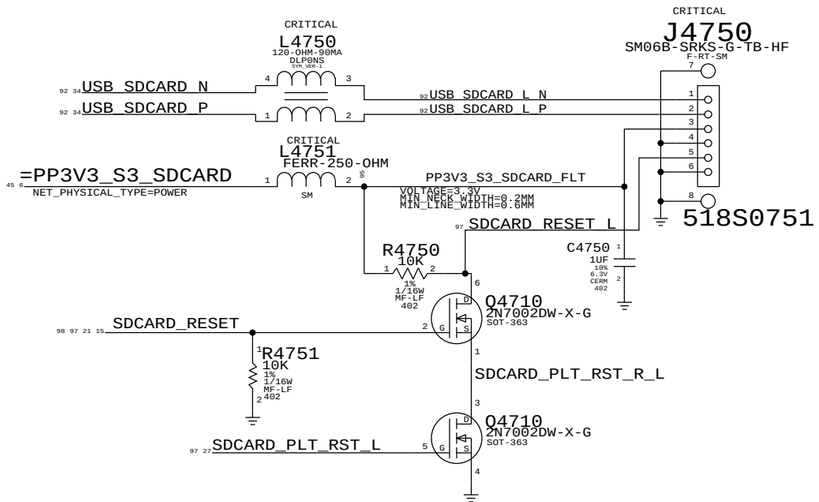


CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



Skin Temp sense at upper Left Screen corner

SD Card Reader Board (Lazarus)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

Internal USB Connections

Apple Inc.

DRAWING NUMBER	051-8115
SIZE	D
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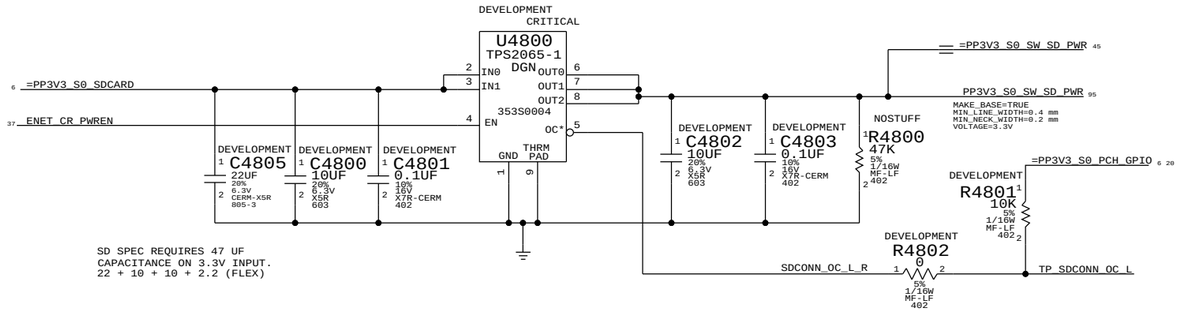
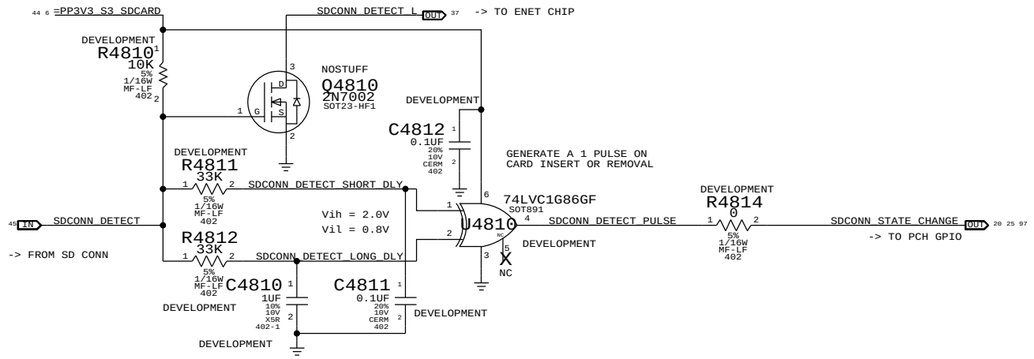
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.

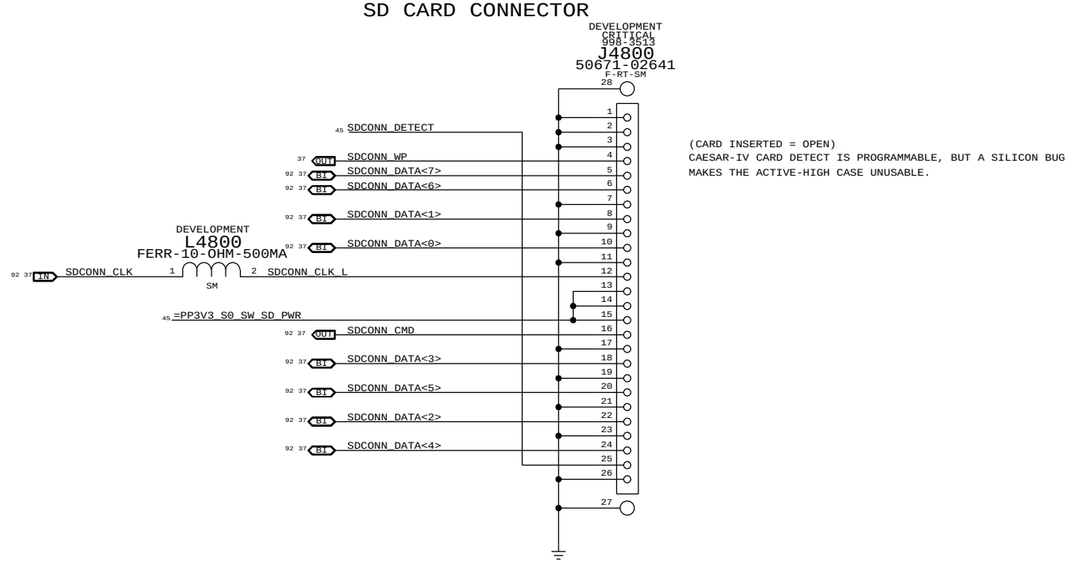


SD SPEC REQUIRES 47 UF
CAPACITANCE ON 3.3V INPUT.
22 + 10 + 10 + 2.2 (FLEX)

SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

47 OUT	SMC_EXCARD_PWR_EN	B12	P10	
47 OUT	SMC_RSTGATE_L	C13	P11	
97 64 IN	ALL_SYS_PWRGD_SMC	A15	P12	
97 64 IN	RSMRST_PWRGD	B14	P13	
	NC	B15	P14	
97 27 OUT	PM_RSMRST_L	C14	P15	
47 OUT	CPUIMVP_VR_ON	D12	P16	
97 25 19 OUT	PM_PWRBTN_L	C15	P17	
K62 NEW:NOT USE	NC	D13	P20	
	NC	D14	P21	
	NC	D15	P22	
	NC	E12	P23	
K62 NEW:NOT USE	NC	E14	P24	
	NC	E15	P25	
K62 NEW:NOT USE	NC	E13	P26	
	NC	F14	P27	
91 48 18 BI	LPC_AD<0>	D9	P30	
91 48 18 BI	LPC_AD<1>	C9	P31	
91 48 18 BI	LPC_AD<2>	A9	P32	
91 48 18 BI	LPC_AD<3>	B9	P33	
91 48 18 IN	LPC_FRAME_L	D8	P34	
97 27 IN	SMC_LRESET_L	C8	P35	
91 27 IN	LPC_CLK33M_SMC	A8	P36	
48 18 BI	LPC_SERIRQ	D7	P37	
	NC	A5	P40	
K62 P1 NOT USED, WAS OOB_TEMP	NC	B5	P41	
49 BI	SMB_MGMT_DATA	D5	P42 (OC)	
47 OUT	SMS_ONOFF_L	C3	P43	
	NC	B1	P44	
	NC	C2	P45	
47 OUT	SMC_GFX_THROTTLE_L	D3	P46	
	NC	C1	P47	
48 47 46 43 OUT	SMC_TX_L	G1	P50	
48 47 46 43 IN	SMC_RX_L	G4	P51	
49 BI	SMB_0_S0_CLK	F2	P52 (OC)	

P60	L13	SMC_PM_G2_EN	OUT	19 74 97
P61	L14	NC		
P62	L15	NC		
P63	K12	NC		
P64	K13	SMC_ADAPTER_EN	OUT	19 47 97
P65	K14	NC		
P66	J12	SMC_PROCHOT_3_3_L	IN	47 97
P67	J13	SMC_BIL_BUTTON_L	IN	47
P70	N12	SMC_VCORE_ISENSE	IN	50 94 (IMON)
P71	R13	SMC_VCORE_VSENSE	IN	50 94 (IMON)
P72	P13	SMC_CPU_1V5_ISENSE	IN	50 94
P73	R14	SMC_CPU_1V5_VSENSE	IN	50 94
P74	P14	SMC_VCCSA_ISENSE	IN	50 94
P75	R15	SMC_VCCSA_VSENSE	IN	50 94
P76	N13	SMC_VAXG_ISENSE	IN	50 94 (IMON)
P77	P15	SMC_VAXG_VSENSE	IN	50 94 (IMON)
P80	C7	SMC_WAKE_SCI_L	OUT	15 18 21 97 PROTO-3, Change back to WAKE_SCI_L
P81	A7	NC		
P82	B7	PM_CLKRUN_L	OUT	15 19 48 97
P83	D6	LPC_PWRDWN_L	IN	19 48 97
P84	C6	SMC_TX_L	OUT	43 46 47 48
P85	A6	SMC_RX_L	IN	43 46 47 48
P86	B6	(OC) SMB_MGMT_CLK	BI	49
P90	K4	SMC_ONOFF_L	IN	47 97
P91	J2	SMC_BC_ACOK	IN	47
P92	J1	NC		
P93	J3	PM_SLP_S3_L	IN	5 19 26 32 36 47 63 82 97
P94	J4	PM_SLP_S4_L	IN	5 19 32 47 53 97 K60 New Change
P95	H2	PM_SLP_S5_L	IN	5 19 47 63 97 K60 New Change
P96	H1	PM_CLK32K_SUSCLK	IN	9 91 97
P97	G2	(OC) SMB_0_S0_DATA	BI	49

U4900
H8S2117
LFBGA
(2 OF 4)
OMIT

K62 NEW:NOT USE,PULLED UP	47 IN	SMC_PA0	R3	PA0
	97 18 OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)	P3	PA1
	97 27 25 19 OUT	PM_SYSRST_L (OC)	R2	PA2
	47 43 OUT	USB_DEBUGPRT_EN_L (OC)	N3	PA3
	47 IN	MEM_EVENT_A_L (OC)	R1	PA4
	47 IN	MEM_EVENT_B_L (OC)	N2	PA5
	47 BI	SYS_ONEWIRE (OC)	M4	PA6
	97 19 15 OUT	PM_BATLOW_L (OC)	N1	PA7
	NC		B10	PB0
PROTO-3:back to K75F	97 47 23 OUT	SMC_RUNTIME_SCI_L	A10	PB1
	98 42 IN	SMC_ODD_DETECT	D10	PB2
K62 NEW:NOT USE,PULLED UP	47 IN	(See below) SMC_PB3	A11	PB3
	94 51 IN	SMC_HDD_OOB_TEMP	B11	PB4
	NC		C11	PB5
K62 NEW:NOT USE,PULLED UP	IN	SMC_PB6	A12	PB6
	47 IN	SMC_GFX_OVERTEMP_L	D11	PB7
	53 OUT	SMC_FAN_0_CTL	G14	PC0
	53 OUT	SMC_FAN_1_CTL	G15	PC1
	NC		G13	PC2
	54 OUT	SMC_FAN_3_CTL	G12	PC3
	53 IN	SMC_FAN_0_TACH	H14	PC4
	53 IN	SMC_FAN_1_TACH	H15	PC5
	NC		H13	PC6
	54 IN	SMC_FAN_3_TACH	H12	PC7
(IMON)	94 50 IN	SMC_1V05_ISENSE	M11	PD0
(IMON)	94 50 IN	SMC_1V05_VSENSE	P11	PD1
	94 50 IN	SMC_PCH_1V05_ISENSE	R11	PD2
	94 50 IN	SMC_PCH_1V05_VSENSE	N11	PD3
	94 50 IN	SMC_GPU_ISENSE	P10	PD4
	94 50 IN	SMC_GPU_VSENSE	R10	PD5
	94 50 IN	SMC_DIMM_ISENSE	N10	PD6
	94 50 IN	SMC_DIMM_VSENSE	M10	PD7

PE0	M3	SMC_PE0	IN	47 K62 NEW:NOT USE,PULLED UP
PE1*	M2	SMC_TCK	IN	47 48
PE2*	M1	SMC_TDI	IN	47 48
PE3*	L4	SMC_TDO	OUT	47 48
PE4*	L2	SMC_TMS	IN	47 48
PF0	M7	G3_POWERON_L	IN	47
PF1	P6	SMC_SYS_LED	OUT	47
PF2	R6	SMC_LID		47
PF3	N6	NC		
PF4	M6	NC		
PF5	R5	BDV_BKL_PWM	OUT	83 97 K62 PROTO-2:NEW
PF6	P5	NC		
PF7	N5	NC		
PG0	P9	NC		
PG1	R9	SMC_SMS_INT	IN	47
PG2	N9	(OC) SMB_BSA_DATA	BI	49
PG3	P8	(OC) SMB_BSA_CLK	BI	49
PG4	R8	(OC) SMB_A_S3_DATA	BI	49
PG5	M8	(OC) SMB_A_S3_CLK	BI	49
PG6	P7	(OC) SMB_B_S0_DATA	BI	49
PG7	R7	(OC) SMB_B_S0_CLK	BI	49
PH0	E1	SMC_PROCHOT	OUT	47 97
PH1	F3	SMC_THRMTRIP	OUT	
PH2	K2	NC		
PECI	PH3 C4	97 CPU_PECI_R		
PEVref	PH4 D4	PVCCIO_S0_SMC_R		
PEVSTP	PH5 B3	97 PM_PECI_PWRGD_R		

R4910 0 MF-LF 5% 1/16W 402 — CPU_PECI 11 21 97
R4911 0 MF-LF 5% 1/16W 402 — =PPVCCIO_S0_SMC 6 47
R4912 0 MF-LF 5% 1/16W 402 — PM_PECI_PWRGD 64 97
C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

95 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

R4999 4.7 5% 1/16W MF-LF 402 — Peak/Ave/Standby= 2mA/1mA/5uA
95 46 PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

C4907 0.47UF 10% 6.3V CERM-XSR 402
C4920 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
LFBGA
(3 OF 4)
OMIT

97 48 47 IN	SMC_RESET_L	E3	RES*	
94 47	SMC_XTAL	A2	XTAL	
94 47	SMC_EXTAL	B2	EXTAL	
		MD1	E2	SMC_MD1 IN 48
		MD2	K1	SMC_KBC_MDE
		NMI	F4	SMC_NMI IN 48
		ETRST*	L1	SMC_TRST_L IN 48
		AVSS	R12	NOSTUFF

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402
XW4900 SM

95 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
95 46 PP3V3_G3H_SMC_AVCC
GND_SMC_AVSS 46 47 50 94

U4900
H8S2117
LFBGA
(4 OF 4)
OMIT

E4		PJ0	C5 NC
N4		PJ1	B8 NC
M9		PJ2	C10 NC
M12	NC	PJ3	C12 NC
M13		PJ4	A14 NC
L12		PJ5	F15 NC
A3		PJ6	J14 NC
		PJ7	K15 NC
		PI0	N8 NC
		PI1	N7 NC
		PI2	M5 NC
		PI3	L3 NC
		PI4	K3 NC
		PI5	H3 NC
		PI6	H4 NC
		PI7	G3 NC

94 50 47 46 GND_SMC_AVSS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011
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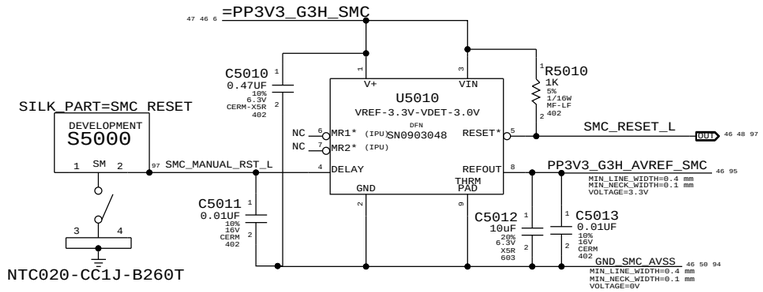
SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L — MXM_ALERT_L (MAKE_BASE=TRUE)
SMC_GFX_THROTTLE_L — MXM_PWR_LEVEL (MAKE_BASE=TRUE)
CPUIMVP_VR_ON — SMC_DELAYED_PWRGD (MAKE_BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

=PP3V3_G3H_SMC

SMC_ONOFF_L	R5020	10K	5% 1/16W MF-LF 402
SMC_TX_L	R5021	10K	5% 1/16W MF-LF 402
SMC_RX_L	R5022	100K	5% 1/16W MF-LF 402
SYS_ONEWIRE	R5023	2.0K	5% 1/16W MF-LF 402
SMC_TMS	R5024	10K	5% 1/16W MF-LF 402
SMC_TDO	R5025	10K	5% 1/16W MF-LF 402
SMC_TDI	R5026	10K	5% 1/16W MF-LF 402
SMC_TCK	R5027	10K	5% 1/16W MF-LF 402
SMC_BI_L_BUTTON_L	R5028	10K	5% 1/16W MF-LF 402
SMC_BC_ACOK	R5029	10K	5% 1/16W MF-LF 402
SMC_ADAPTER_EN	R5030	10K	5% 1/16W MF-LF 402
USB_DEBUGPRT_EN_L	R5031	10K	5% 1/16W MF-LF 402
G3_POWERON_L	R5034	10K	5% 1/16W MF-LF 402
SMC_SMS_INT	R5032	10K	5% 1/16W MF-LF 402
SMC_LID	R5033	10K	5% 1/16W MF-LF 402
SMC_PA0	R5037	100K	5% 1/16W MF-LF 402
SMC_PB6	R5038	100K	5% 1/16W MF-LF 402
SMC_PE0	R5036	100K	5% 1/16W MF-LF 402

=PP3V3_S0_SMC_LS

SMC_GFX_OVERTEMP_L	R5035	10K	5% 1/16W MF-LF 402
SMC_RUNTIME_SCI_L	R5044	10K	5% 1/16W MF-LF 402

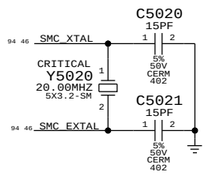
UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN (MAKE_BASE=TRUE)
SMS_ONOFF_L — TP_SMS_ONOFF_L (MAKE_BASE=TRUE)
SMC_RSTGATE_L — TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
SMC_SYS_LED — TP_SMC_SYS_LED (MAKE_BASE=TRUE)
SMC_PB3 — TP_SMC_PB3 (MAKE_BASE=TRUE)

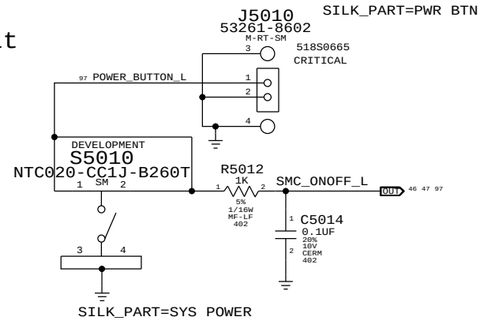
=PP3V3_S0_SMC_LS

PM_SLP_S3_L	R5041	100K	5% 1/16W MF-LF 402
PM_SLP_S5_L	R5042	100K	5% 1/16W MF-LF 402
PM_SLP_S4_L	R5043	100K	5% 1/16W MF-LF 402

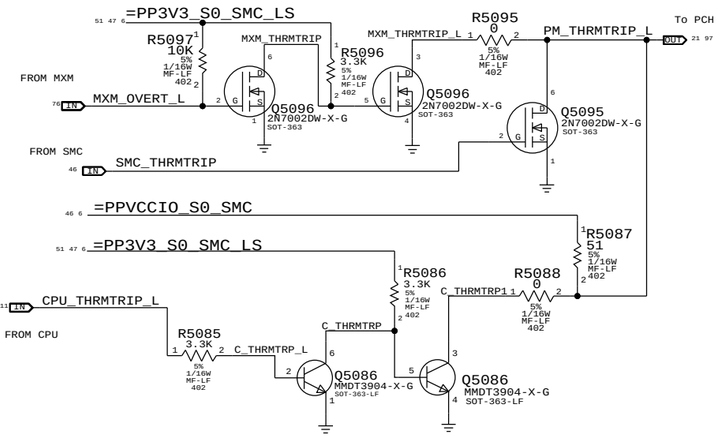
SMC Crystal Circuit



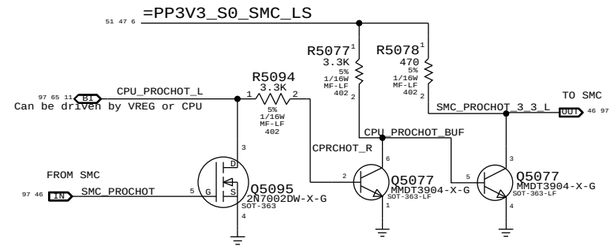
POWER BUTTON



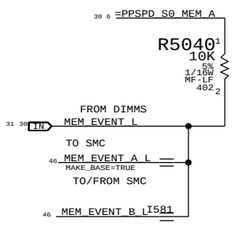
SMC & MXM THERMTRIP LEVEL SHIFTING



SMC PROCHOT 3.3V LEVEL SHIFTING



MEM_EVENT



SYNC_MASTER=K62	SYNC_DATE=01/06/2011
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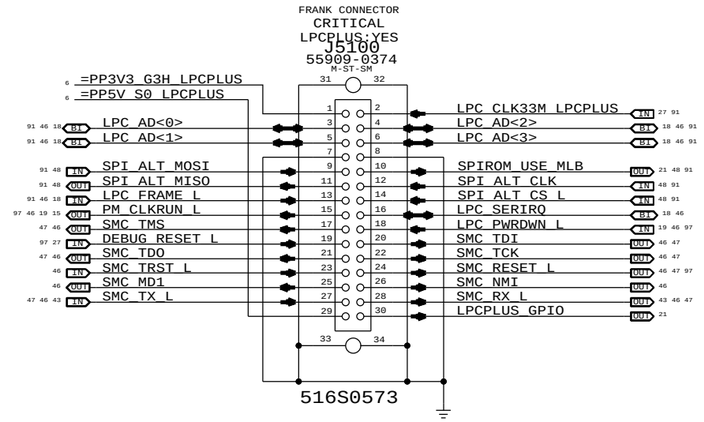
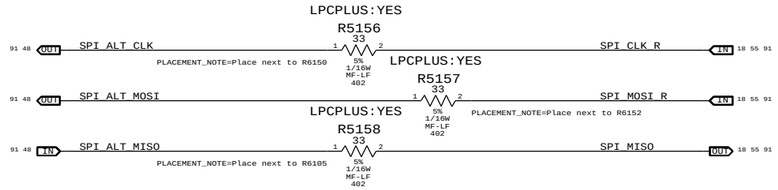
LPC+SPI Connector



Alternate SPI ROM Support

SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

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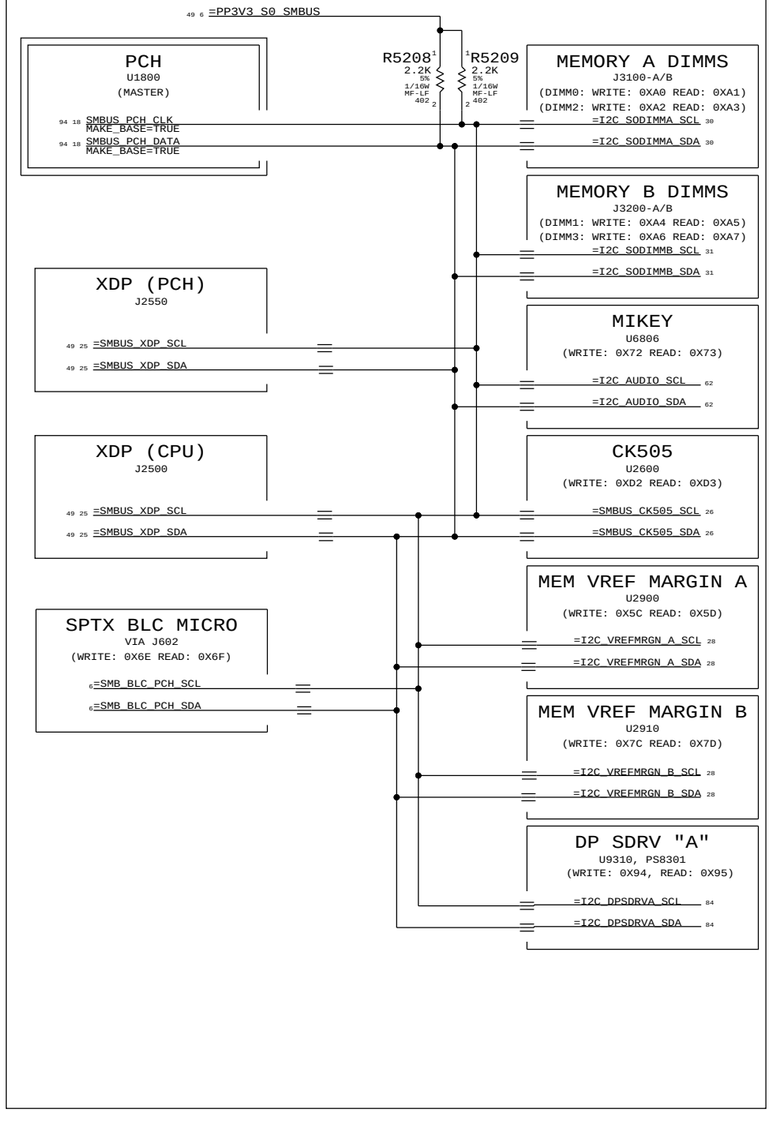
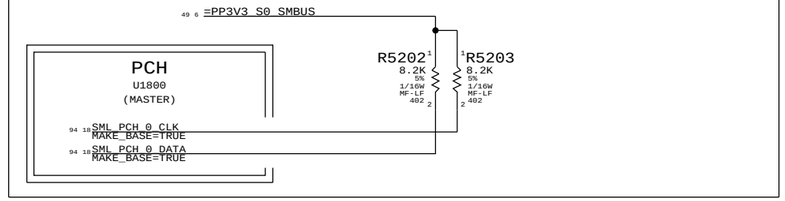
PCH "SMBUS" CONNECTIONS



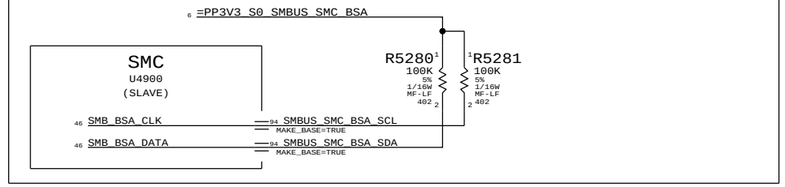
PCH "SML 0" CONNECTIONS



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

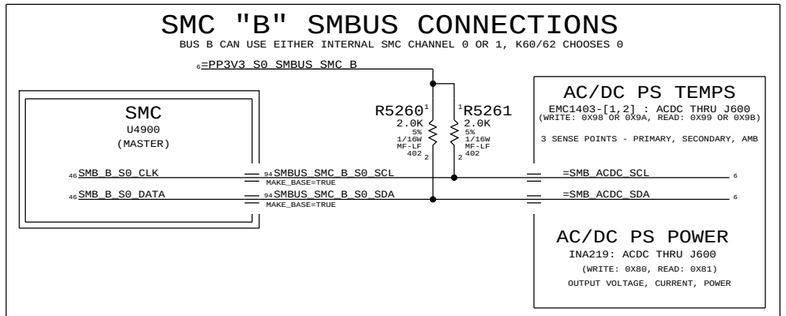
SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)



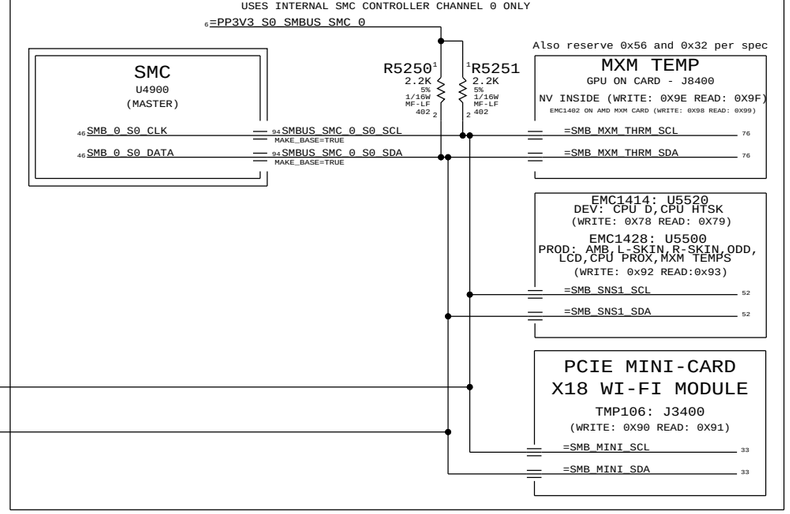
SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

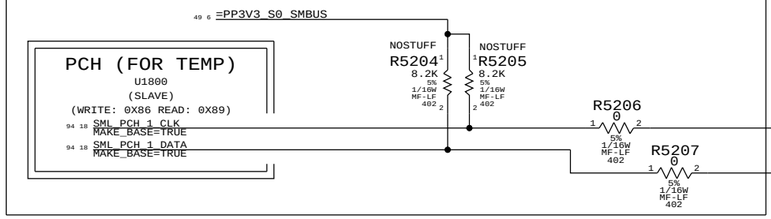


SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY



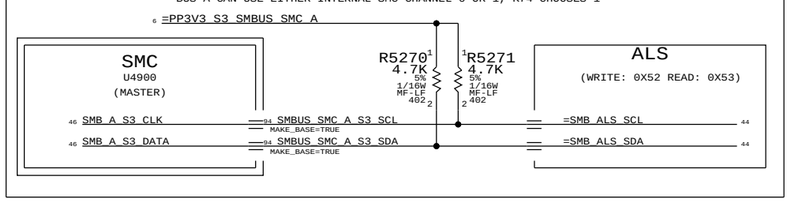
PCH "SML 1" CONNECTIONS



THE PCH address is user programmable by SPI ROM

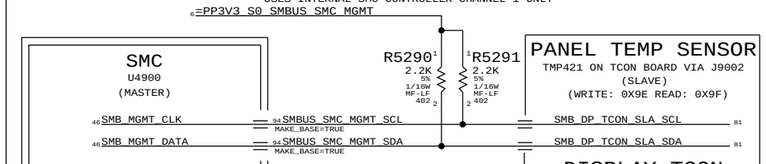
SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

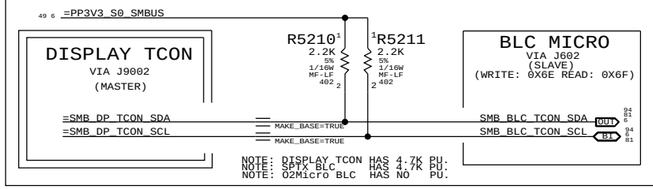


SMC "MANAGEMENT" SMBUS (BUS 1)

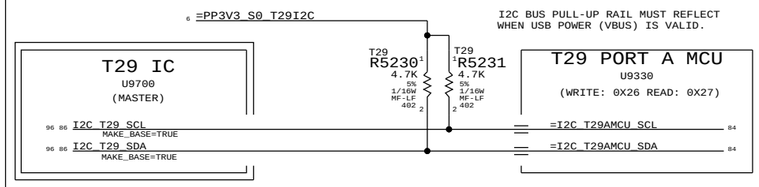
USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY



DISPLAY TCON TO SPTX OR O2M BLC



T29 I2C CONNECTIONS



SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE

SMBUS CONNECTIONS

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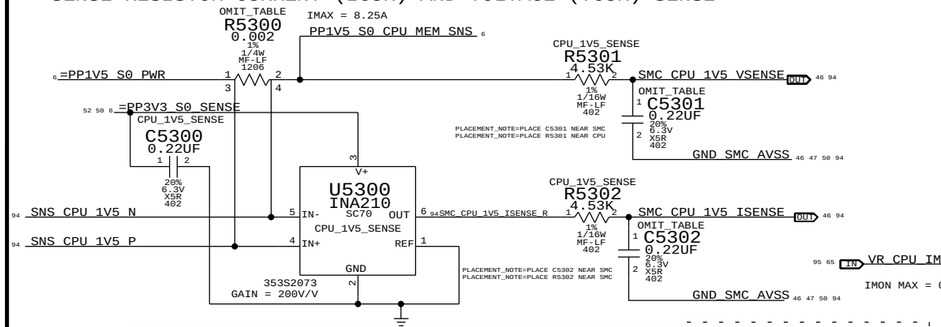
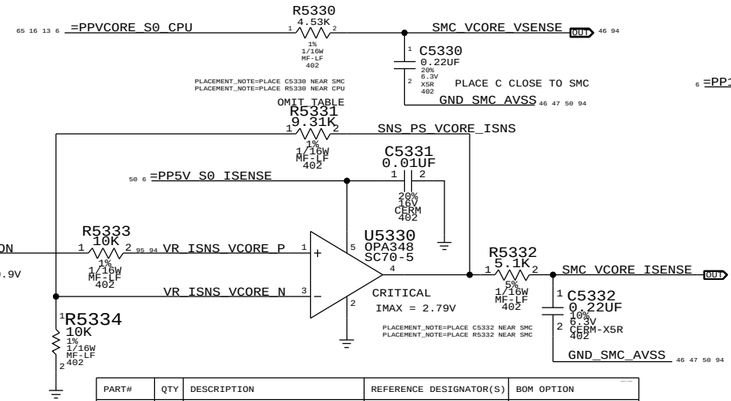
CPU VDD 1.5V
SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

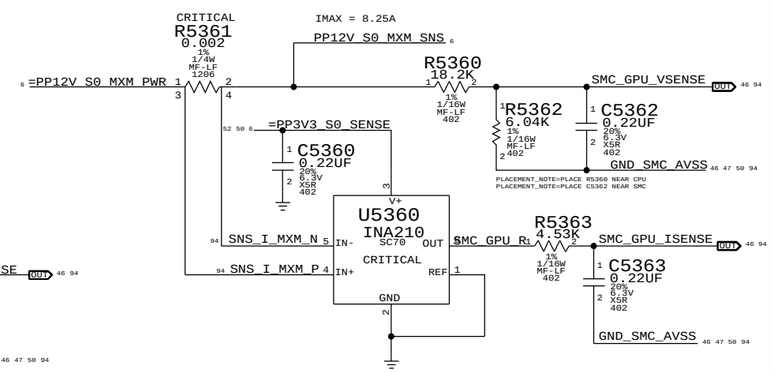
THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE CONFIGURATIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

CPU VCC (VCORE)
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE

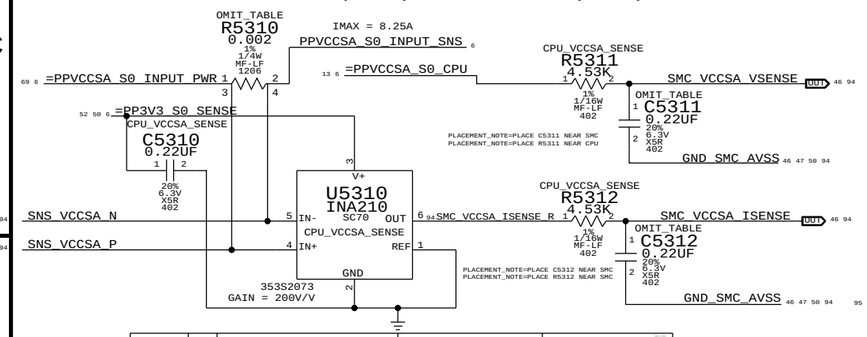


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

GPU MXM
SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE

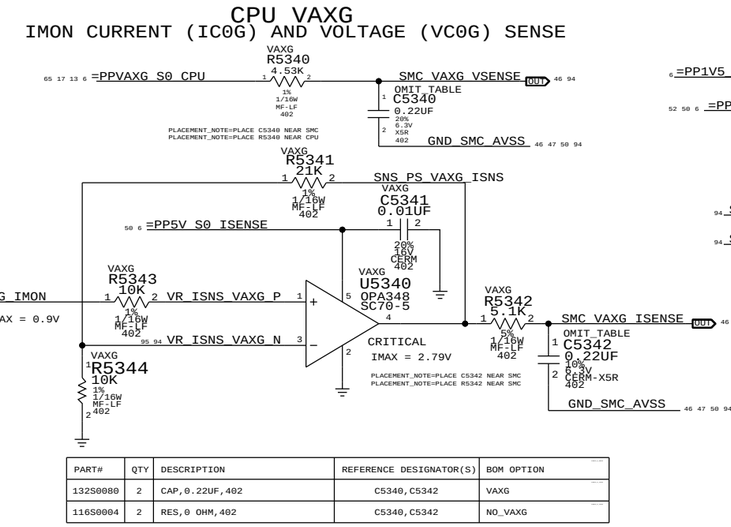


CPU VCCSA
SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



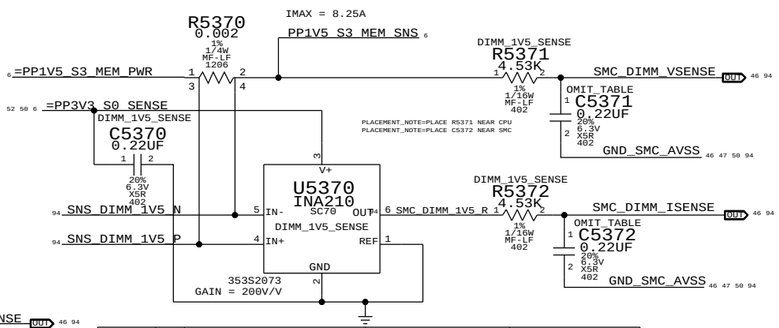
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG
IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



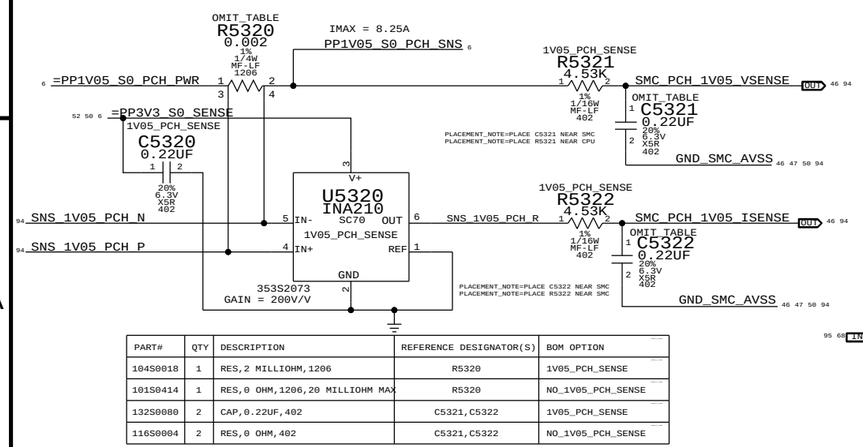
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)
SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



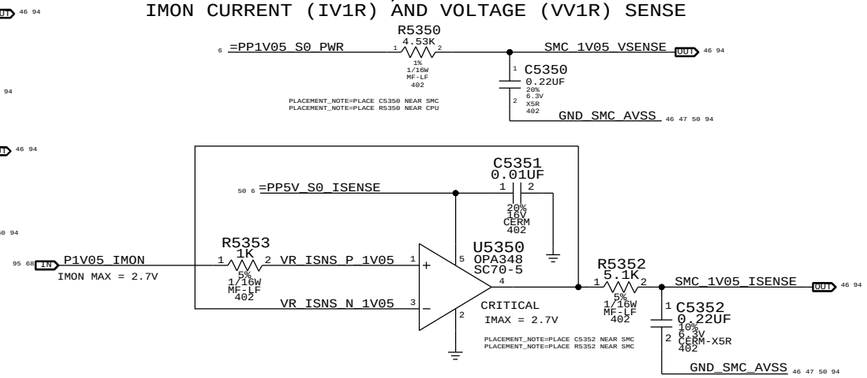
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V
SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V
IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE



NOTE: TOTAL CPU POWER = VC0C+IC0C
+ VC5R*IC5R
+ VCSR*ICSR
+ VC0G*IC0G
+ VV1R*IC1R

where
IC1R = IV1R - IN1R - ICSR

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU/PCH/GPU POWER SENSE

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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BRANCH
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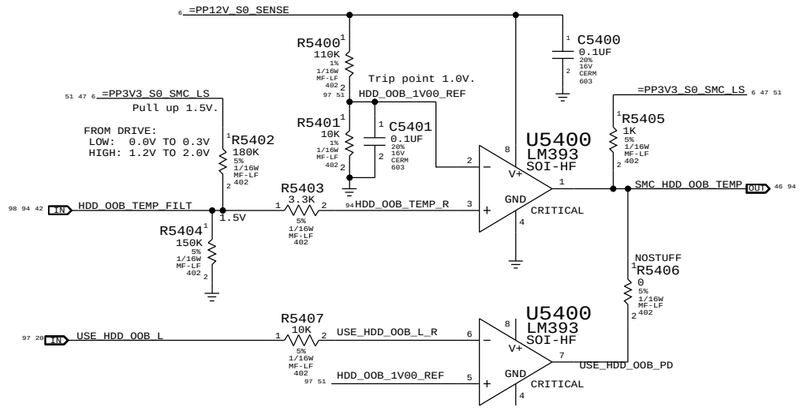
SHEET 50 OF 98

HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
HDD OOB SENSE

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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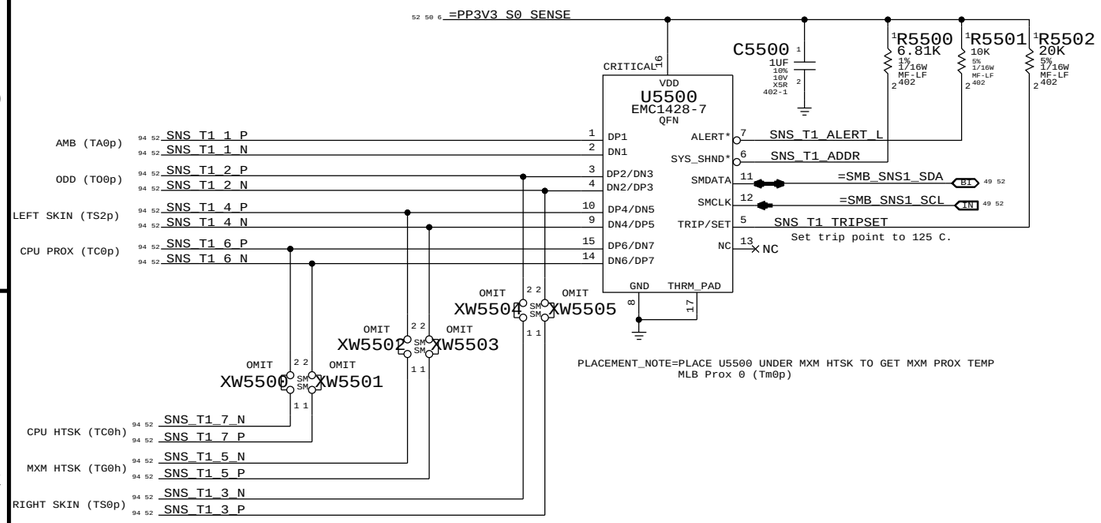
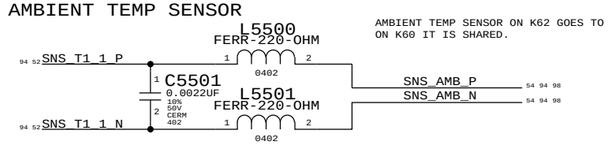
SNS T1: PRODUCTION TEMP SENSOR IC



PLACEMENT_NOTE=PLACE U5500 UNDER MXM HTSK TO GET MXM PROX TEMP
MLB Prox 0 (Tm0p)

EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

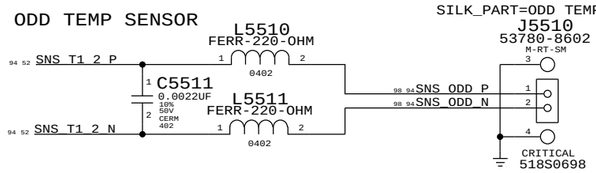
AMBIENT TEMP SENSOR



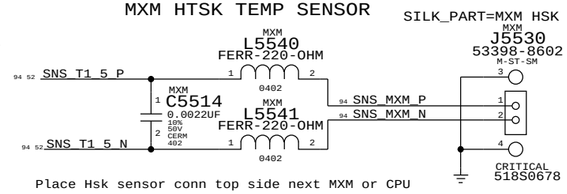
AMBIENT TEMP SENSOR ON K62 GOES TO J5500.
ON K60 IT IS SHARED.

518S0677

ODD TEMP SENSOR

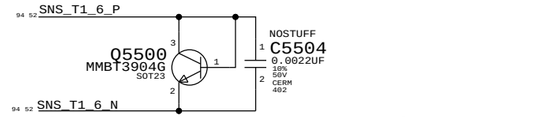


MXM HTSK TEMP SENSOR



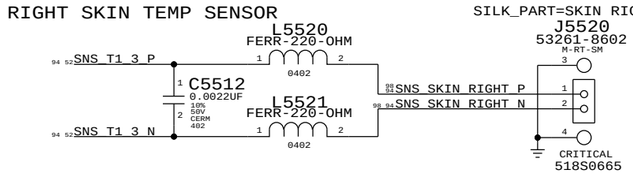
Place Hsk sensor conn top side next MXM or CPU

CPU PROXIMITY TEMP SENSOR

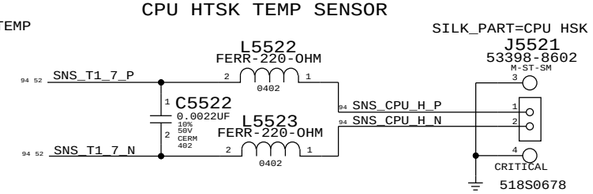


Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

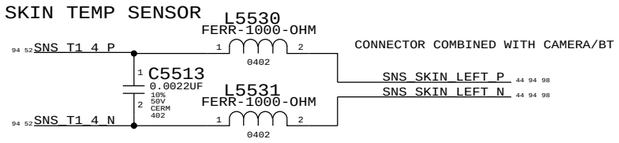
RIGHT SKIN TEMP SENSOR



CPU HTSK TEMP SENSOR



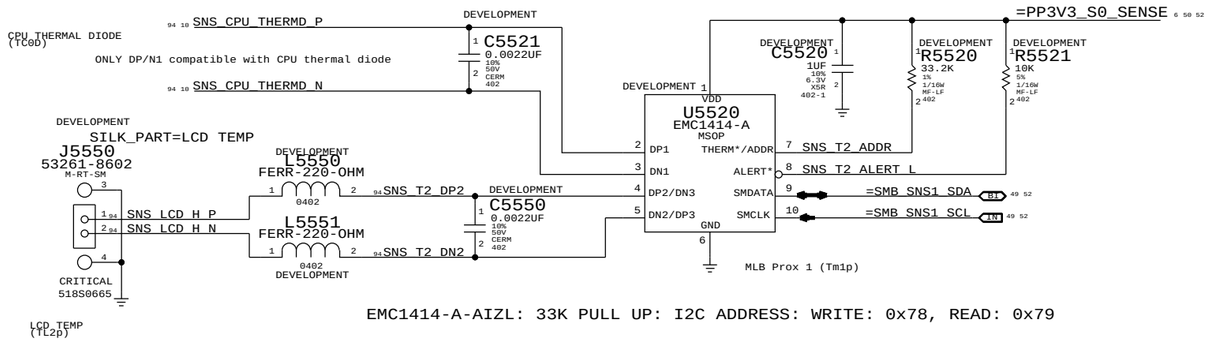
LEFT SKIN TEMP SENSOR



CONNECTOR COMBINED WITH CAMERA/BT

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



MLB Prox 1 (Tm1p)

EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE: TEMP SENSORS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
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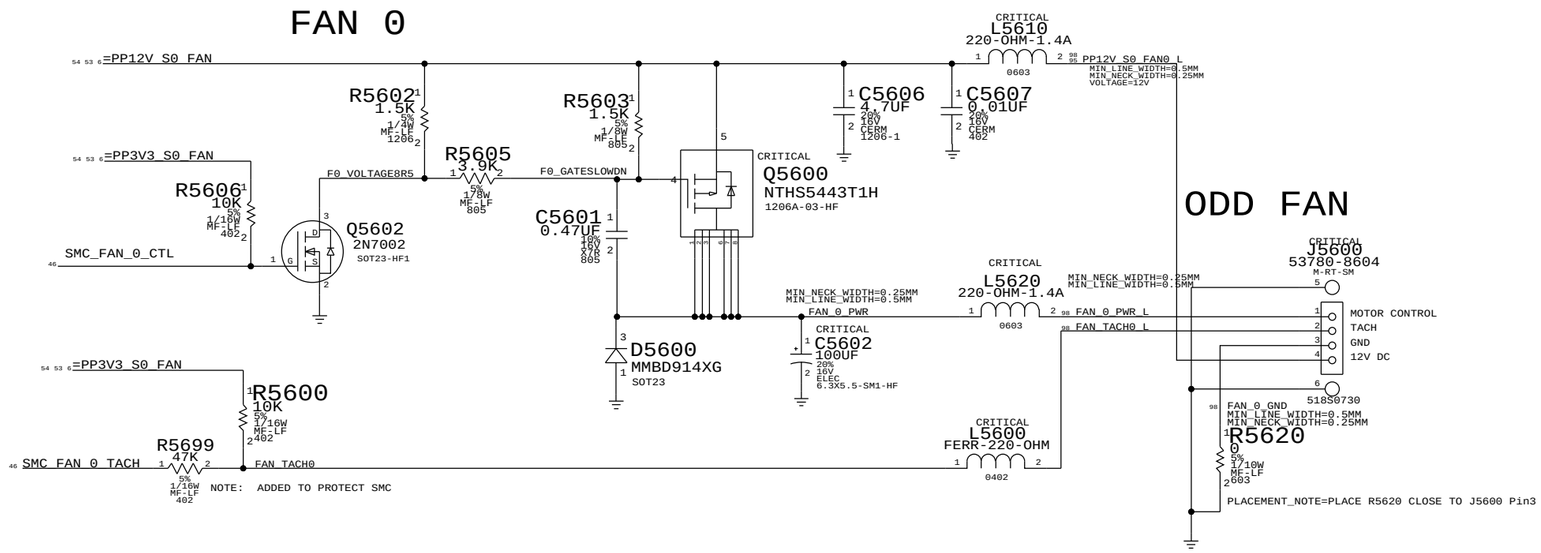

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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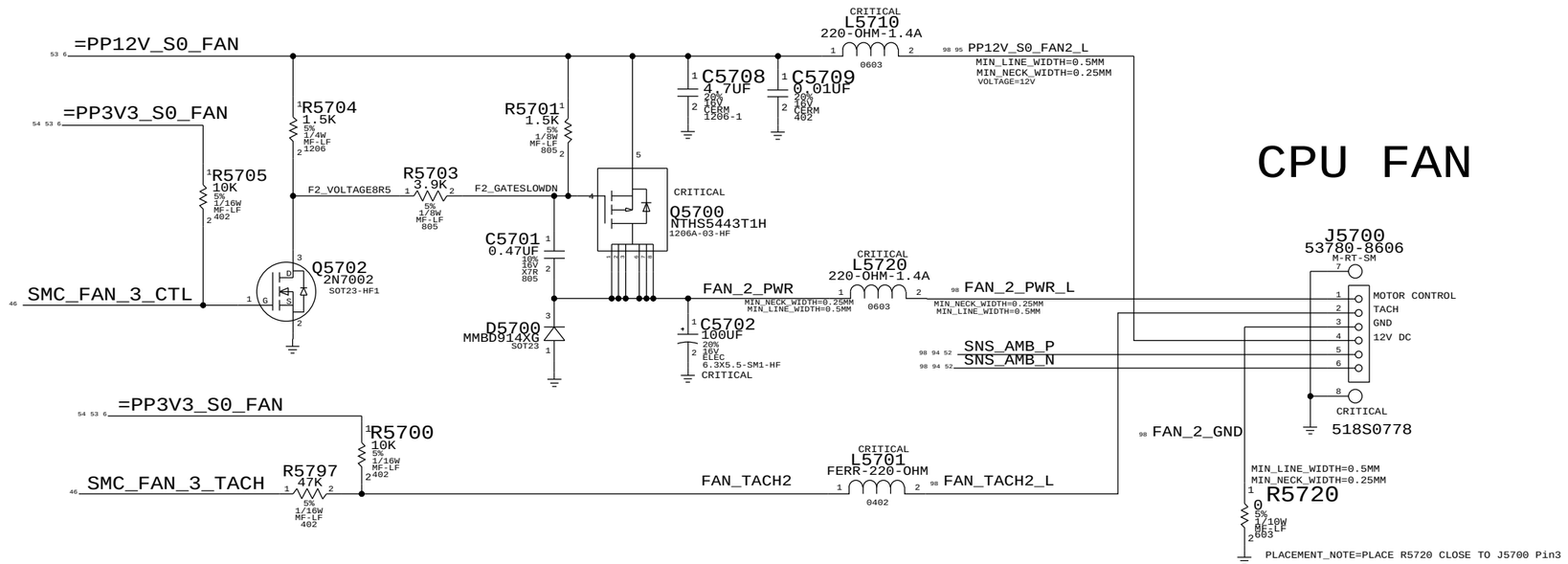
SMC'S FAN3 OUTPUT CONTROL FAN 2



CPU FAN

FAN 3 SMC CONTROL (UNUSED)

SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE: CPU FAN

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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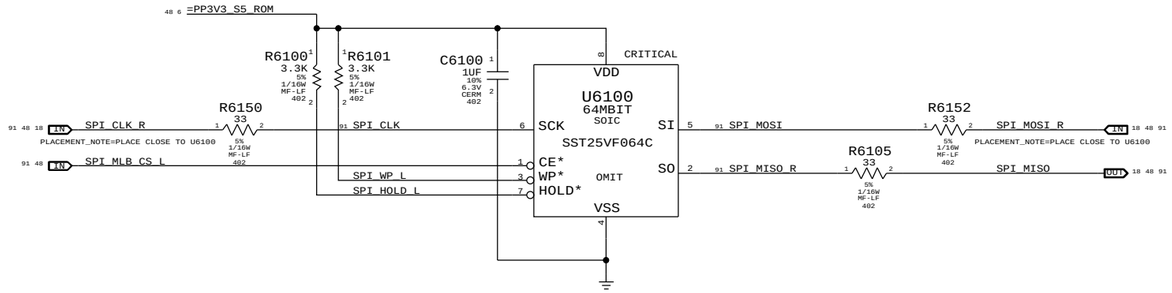

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

SPI ROM

Apple Inc.

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REVISION 11.1.0

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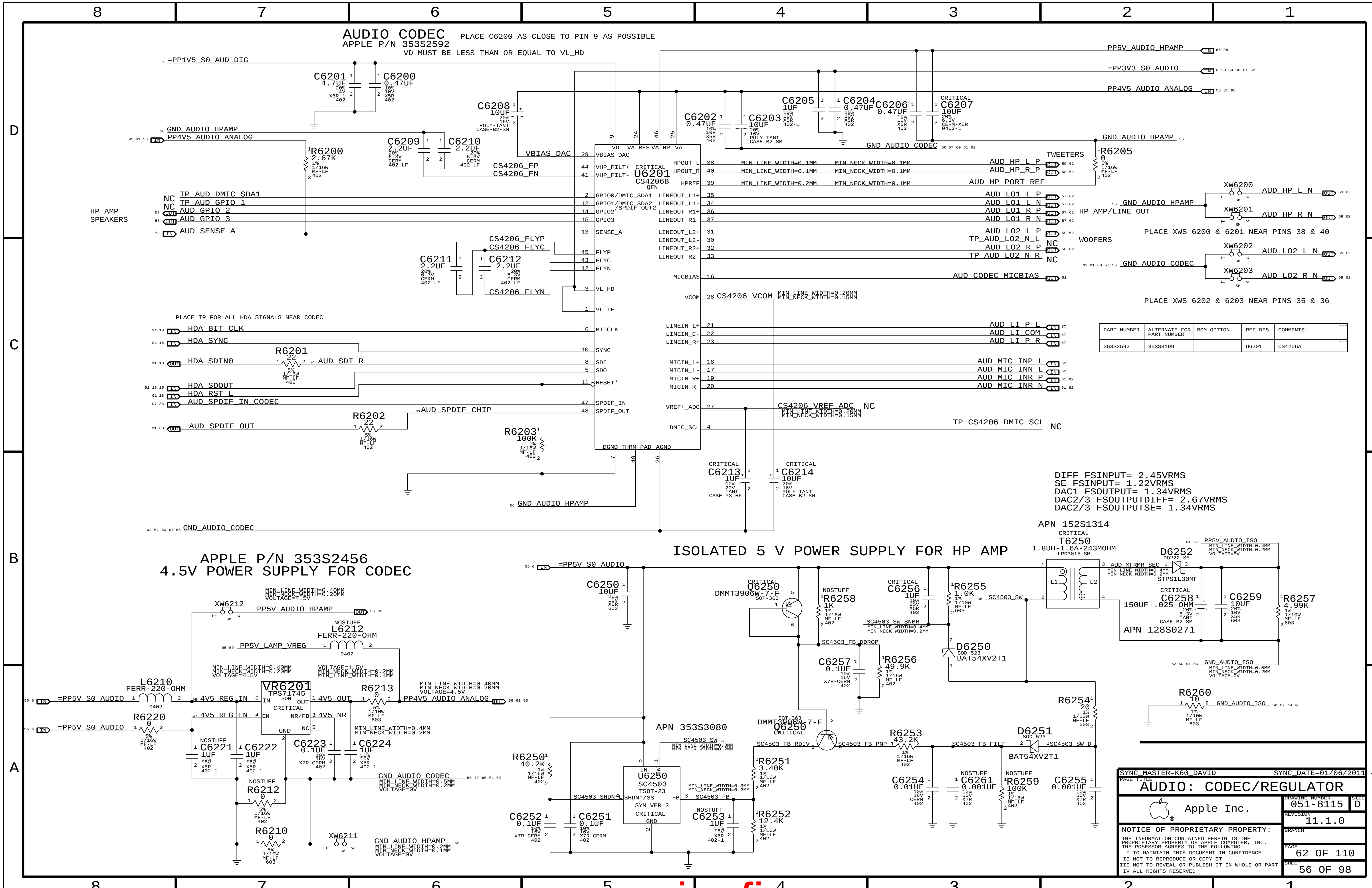

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH

R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY
C6362 220PF 5% 25V CERM 402
R6362 7.87K 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY

62 56 IN AUD_LO1_R_N → CRITICAL C6361 33UF 20% 6.3V TANT CASE-A → AUD_LO1_R_C_N → R6361 10K 1% 1/16W MF-LF 402 → MAX97220_INR_N OUT 57 62

62 56 IN AUD_LO1_R_P → CRITICAL C6363 33UF 20% 6.3V TANT CASE-A → AUD_LO1_R_C_P → R6363 10K 1% 1/16W MF-LF 402 → MAX97220_INR_P OUT 57 62

SIGNAL_MODEL=EMPTY R6364 7.87K 1% 1/16W MF-LF 402 — C6364 220PF 5% 25V CERM 402 SIGNAL_MODEL=EMPTY

62 60 57 56 GND_AUDIO_ISO — R6365 0 5% 1/16W MF-LF 402 — MAX97220_SGND

SIGNAL_MODEL=EMPTY R6374 7.87K 1% 1/16W MF-LF 402 — C6374 220PF 5% 25V CERM 402 SIGNAL_MODEL=EMPTY

62 56 IN AUD_LO1_L_P → CRITICAL C6373 33UF 20% 6.3V TANT CASE-A → AUD_LO1_L_C_P → R6373 10K 1% 1/16W MF-LF 402 → MAX97220_INL_P OUT 57 62

62 56 IN AUD_LO1_L_N → CRITICAL C6371 33UF 20% 6.3V TANT CASE-A → AUD_LO1_L_C_N → R6371 10K 1% 1/16W MF-LF 402 → MAX97220_INL_N OUT 57 62

SIGNAL_MODEL=EMPTY R6372 7.87K 1% 1/16W MF-LF 402 — C6372 220PF 5% 25V CERM 402 SIGNAL_MODEL=EMPTY — MAX97220_OUTL OUT 57 60

61 56 PP5V_AUDIO_ISO

C6350 0.1UF 10% 10V X7R-CERM 402 — C6351 10UF 20% 10V X5R 603

C6352 1UF 10% 10V X5R 402-1 — C6353 1UF 10% 10V X5R 402-1

62 60 57 56 GND_AUDIO_ISO

R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL

L6350 FERR-220-OHM 0402

56 IN AUD_GPIO_2 → R6350 100K 5% 1/16W MF-LF 402 → GND_AUDIO_ISO

U6350 MAX97220AETE TQFN — CRITICAL — PVDD SVDD SVDD2

62 57 IN MAX97220_INR_N → INL-
62 57 IN MAX97220_INR_P → INL+
62 57 IN MAX97220_INL_P → INR+
62 57 IN MAX97220_INL_N → INR-
MAX97220_SHDN_L → SHDN*
PGND SGND PVSS THM_PAD

OUTL → MAX97220_OUTL OUT 57 60 (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM)
BIAS → MAX97220_BIAS (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM)
OUTR → MAX97220_OUTR OUT 57 60 (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM)

C1P → MAX97220_C1P → C6355 1UF 10% 10V X5R 402-1
C1N → MAX97220_C1N (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM) → C6356 1UF 10% 10V X5R 402-1

MAX97220_PVSS (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V) → C6354 1UF 10% 10V X5R 402-1

62 60 57 56 GND_AUDIO_ISO

CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS

60 IN AUD_LI_L (MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM) → R6300 7.87K 1% 1/16W MF-LF 402 (MIN_NECK_WIDTH=.2MM, MIN_LINE_WIDTH=.3MM) → AUD_LI_LF → CRITICAL C6300 22UF 20% 10V TANT SM-HF-PL → AUD_LI_P_L OUT 56 (MIN_NECK_WIDTH=.2MM, MIN_LINE_WIDTH=.3MM)

AUD_LI_LF → R6301 21.5K 1% 1/16W MF-LF 402 — NOSTUFF C6301 820PF 10% 50V CERM 402

60 IN AUD_LI_GND (MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.3MM) → CRITICAL C6302 22UF 20% 10V TANT SM-HF-PL → AUD_LI_COM OUT 56 (MIN_NECK_WIDTH=.3MM, MIN_LINE_WIDTH=.3MM)

AUD_LI_GND → R6303 10 1% 1/16W MF-LF 402 → 62 61 60 56 IN GND_AUDIO_CODEC

AUD_LI_LF → R6305 21.5K 1% 1/16W MF-LF 402 — NOSTUFF C6304 820PF 10% 50V CERM 402

60 IN AUD_LI_R (MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM) → R6306 7.87K 1% 1/16W MF-LF 402 (MIN_NECK_WIDTH=.2MM, MIN_LINE_WIDTH=.3MM) → AUD_LI_RF → CRITICAL C6303 22UF 20% 10V TANT SM-HF-PL → AUD_LI_P_R OUT 56 (MIN_NECK_WIDTH=.2MM, MIN_LINE_WIDTH=.3MM)

SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

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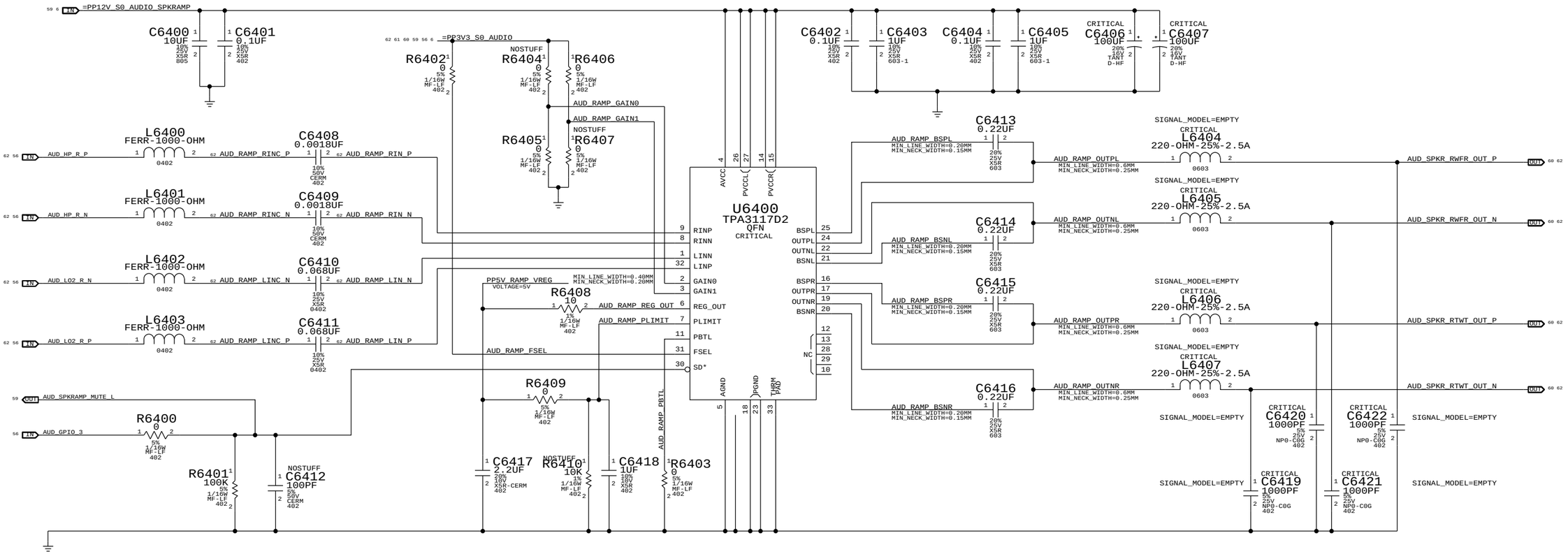
RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID	SYNC_DATE=01/06/2011
PAGE TITLE: AUDIO: SPEAKER AMP_1	
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
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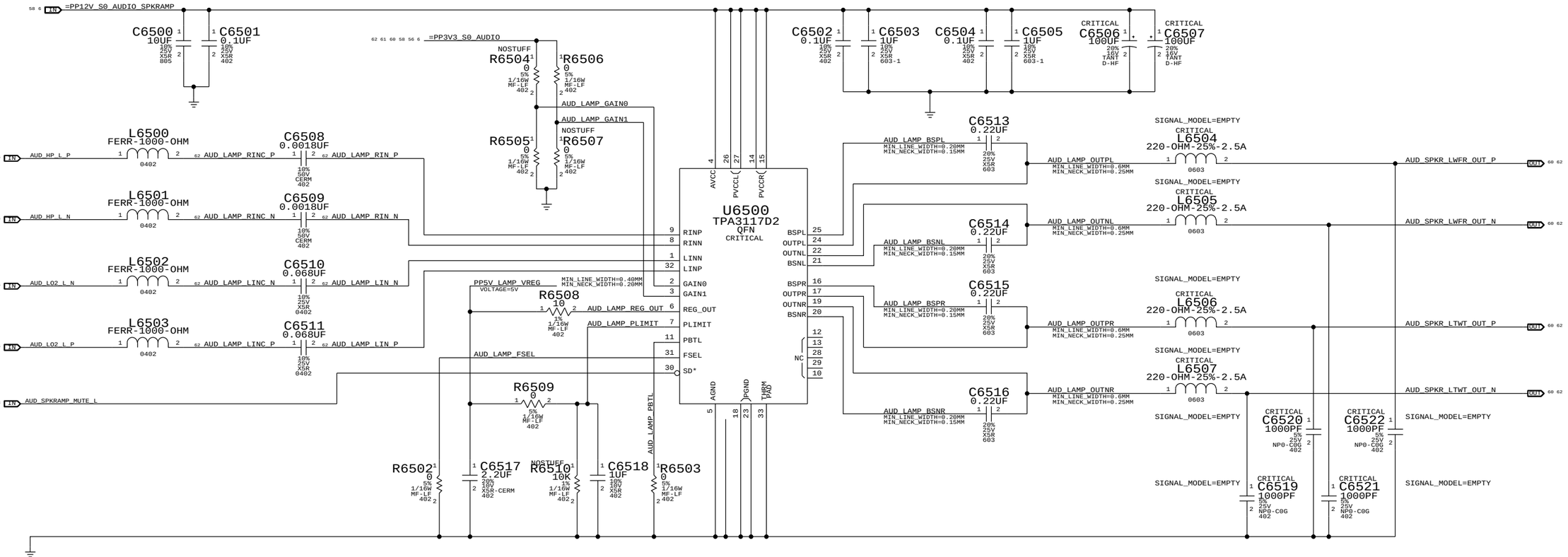
LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID	SYNC_DATE=01/06/2011
PAGE TITLE	AUDIO: SPEAKER AMP
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
	REVISION 11.1.0
	BRANCH
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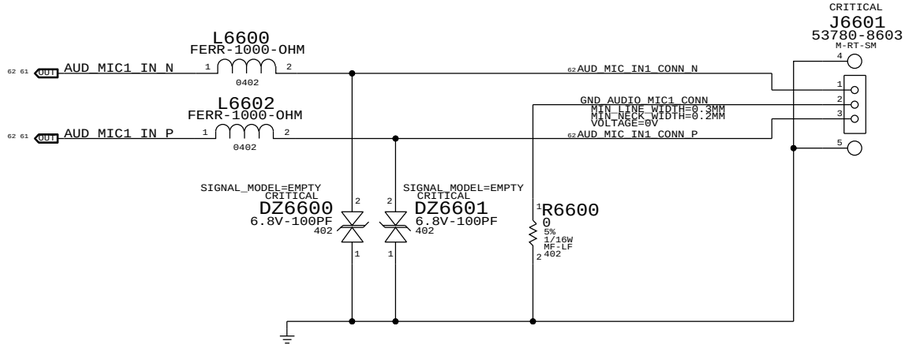
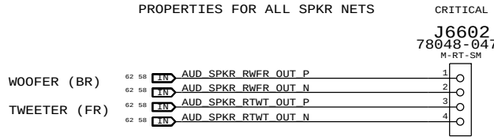
INTERNAL MIC CON
APPLE P/N 518S0677

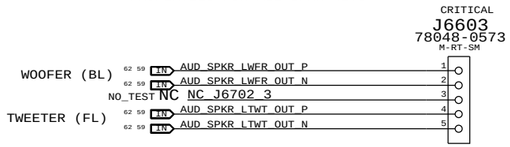


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

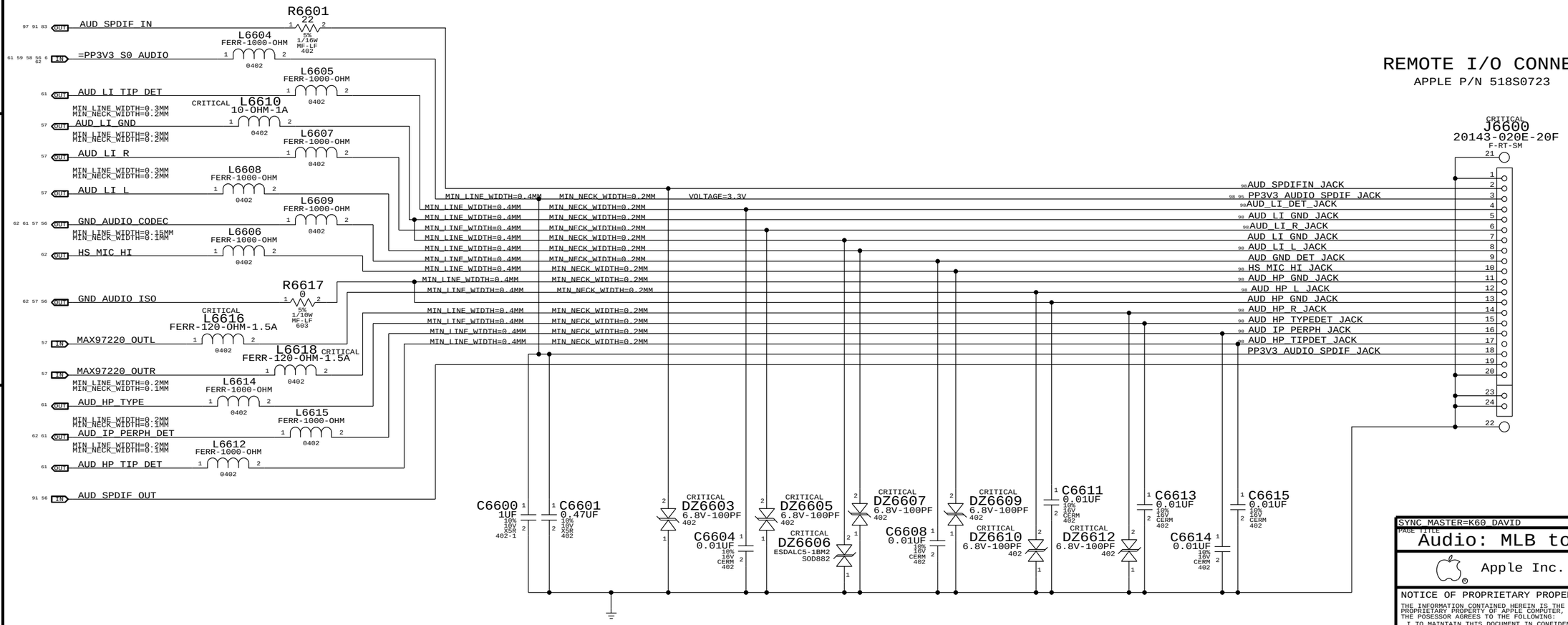
PROPERTIES FOR ALL SPKR NETS



PROPERTIES FOR ALL SPKR NETS



REMOTE I/O CONNECTOR
APPLE P/N 518S0723



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

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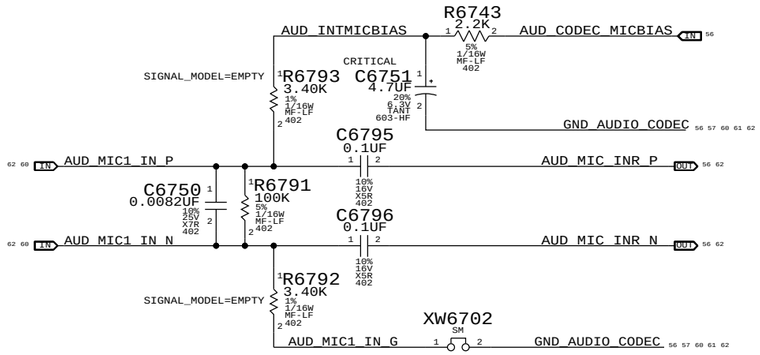
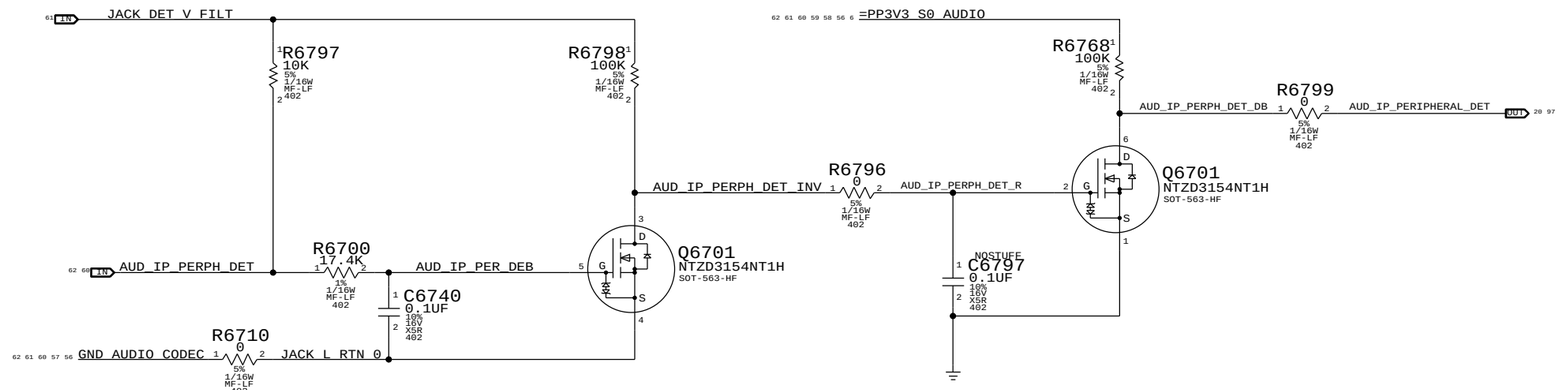
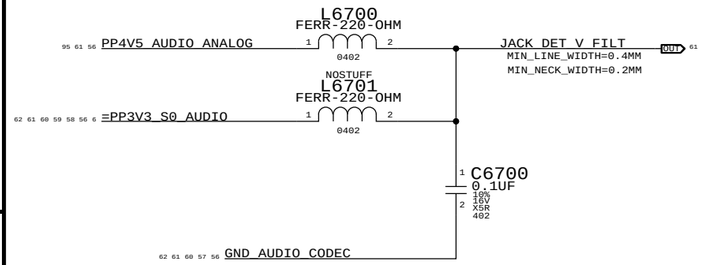
Internal Microphone Impedance Matching



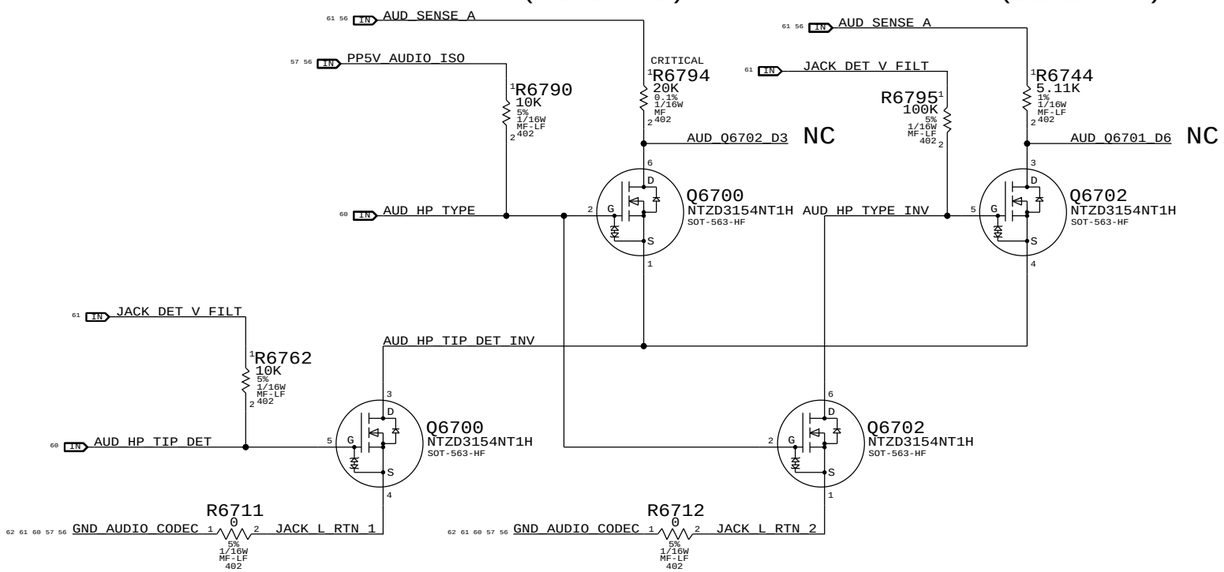
IPHS HS Detect Debounce CKT



L6700 / L6701

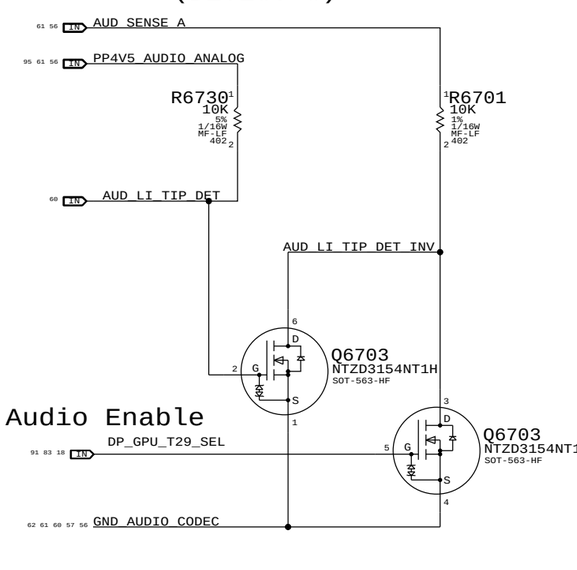


Digital Out (DETECT B)



Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



DP Audio Enable

SYNC_MASTER=K60_DAVID SYNC_DATE=11/24/2010

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (RCVR_INT) COUGAR POINT GPIO 3 (PERIPH_DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

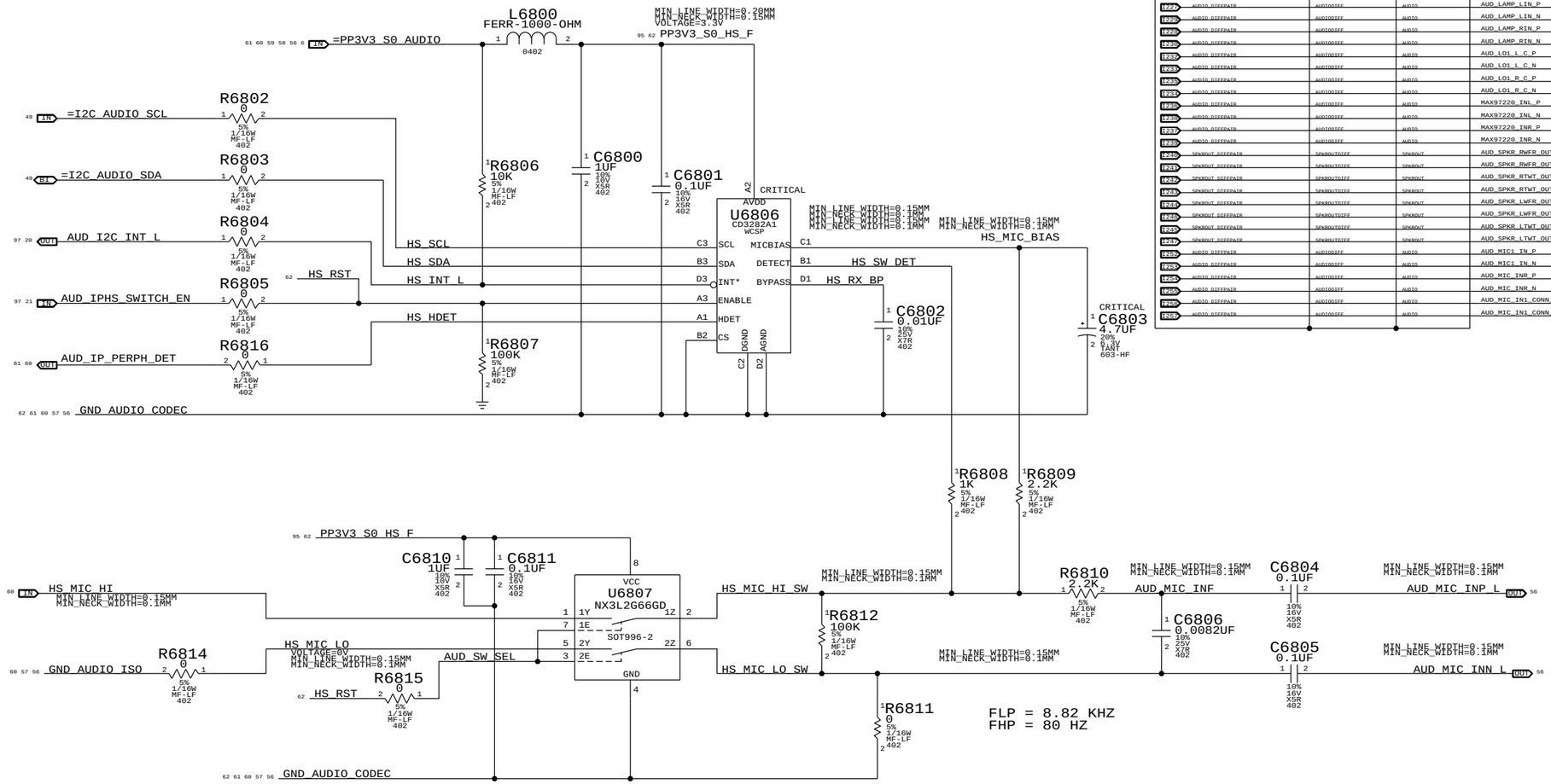
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE

AUDIO: Mikey

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SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
PM_EN_DDRVTT_S0_REG
NOSTUFF C6953 0.1UF 10% 10V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT-363-LF
R6950 10K 5% 1/16W MF-LF 402
PM_PGOOD_P1V05_S0_REG
CPUVTT_REG_PGOOD_R
Q6911 SOT-363-LF MMDT3904-X-G
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
C6910 0.1UF 20% 10V CERM 402
PM_SLP_S5_L
R6971 0 5% 1/16W MF-LF 402
NOSTUFF R6972 0 5% 1/16W MF-LF 402
PM_SLP_S4_L
PM_SLP_S4_1_L_R
U6900 08 74LVC08 TSSOP-HF
S4_ENABLES
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S3_FET
Enable FET
PM_EN_P5V_S3_REG
ENABLE REGULATOR
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
CPU_SKTOCC_L
Q6910 2N7002 SOT23-HF1
NOSTUFF R6917 10K 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

PM_PGOOD_P5V_S3_REG
R6970 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
PM_SLP_S4_L
U6900 08 74LVC08 TSSOP-HF
PM_EN_DDR1V5_S3_REG
PM_PGOOD_P5V_S3_REG
NOSTUFF R6931 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
PM_EN_P1V5_S0_FET

SLP_S3 ENABLES

=PP3V3_S5_PWRCTL
R6955 10K 5% 1/16W MF-LF 402
P3V3_S5_PWRCTL_U6900_R
PGOOD_P12V_S0
U6900 08 74LVC08 TSSOP-HF

=PP3V3_S5_PWRCTL
PM_SLP_S3_L
PM_PGOOD_DDR1V5_S3_REG
U6900 08 74LVC08 TSSOP-HF
PM_EN_P12V_S0_FET

NOSTUFF R6946 33 5% 1/16W MF-LF 402
NOSTUFF R6947 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET
Enable FET
PM_EN_P5V_S0_FET
Enable FET
OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)
NOSTUFF R6944 33 5% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
PM_SLP_S3_BUF_L
PM_EN_P1V5_S0_FET
Enable FET
PM_EN_DDRVTT_S0_REG
Enable regulator

=PP12V_S0_PWRCTL
R6934 82K 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
R6935 33K 5% 1/16W MF-LF 402
OPTION TO DELAY 1V8
R6932 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
NOSTUFF R6990 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P1V8_S0_REG
NOSTUFF C6994 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

OPTIONAL SEQUENCE TO DELAY 3V,1V5
R6930 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P3V3_S0_FET
R6933 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P1V5_S0_FET

NOSTUFF R6942 33 5% 1/16W MF-LF 402
Enable regulator
PM_EN_P1V05_S0_REG
NOSTUFF C6942 1UF 10% 6.3V CERM 402
R6936 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
OPTION TO DELAY 1V05

CPUVTT_VREG/ PCH CORE
NOTE: PM_PGOOD_P1V05_S0_REG ENABLES VCCSA REGULATOR CIRCUIT ON PAGE 70
PM_PGOOD_P1V05_S0_REG = =PM_EN_VCCSA_S0_CPU
MAKE_BASE=TRUE

VCCSA REGULATOR
PM_PGOOD_PVCCSA_S0_REG = Enable regulator PM_EN_PVCORE_CPU
MAKE_BASE=TRUE
TO ENABLE OF CPU VCORE

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POWER SEQUENCING ENABLES

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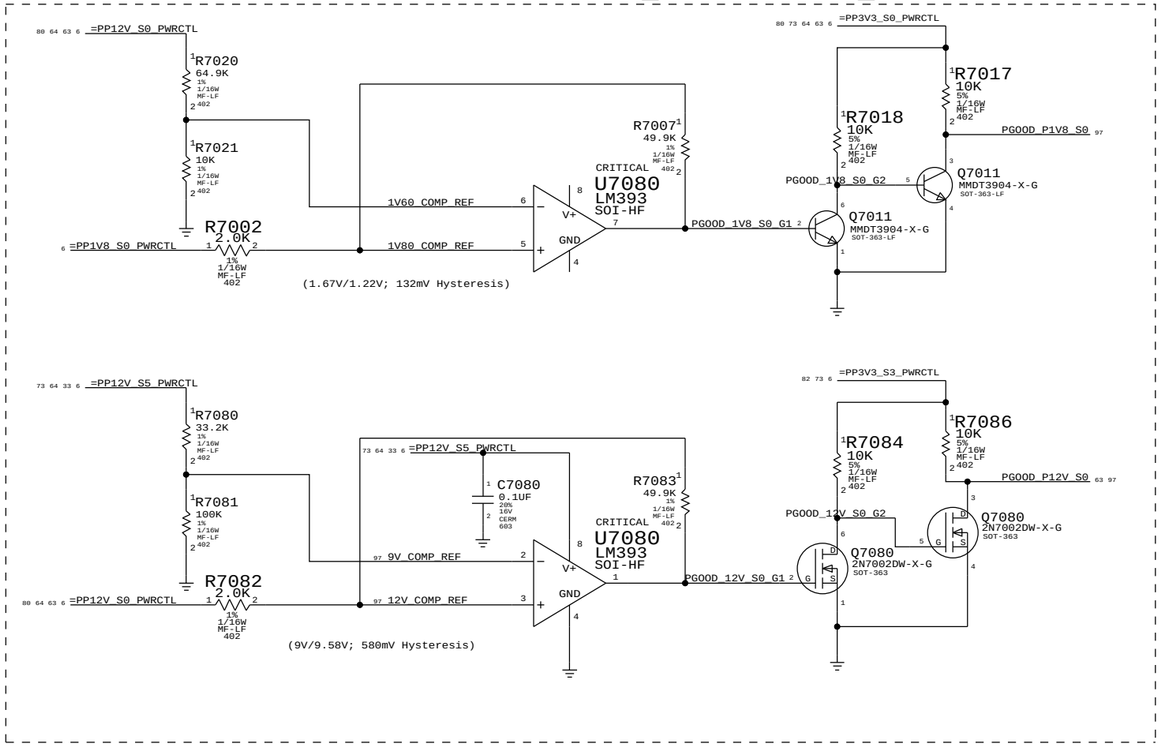
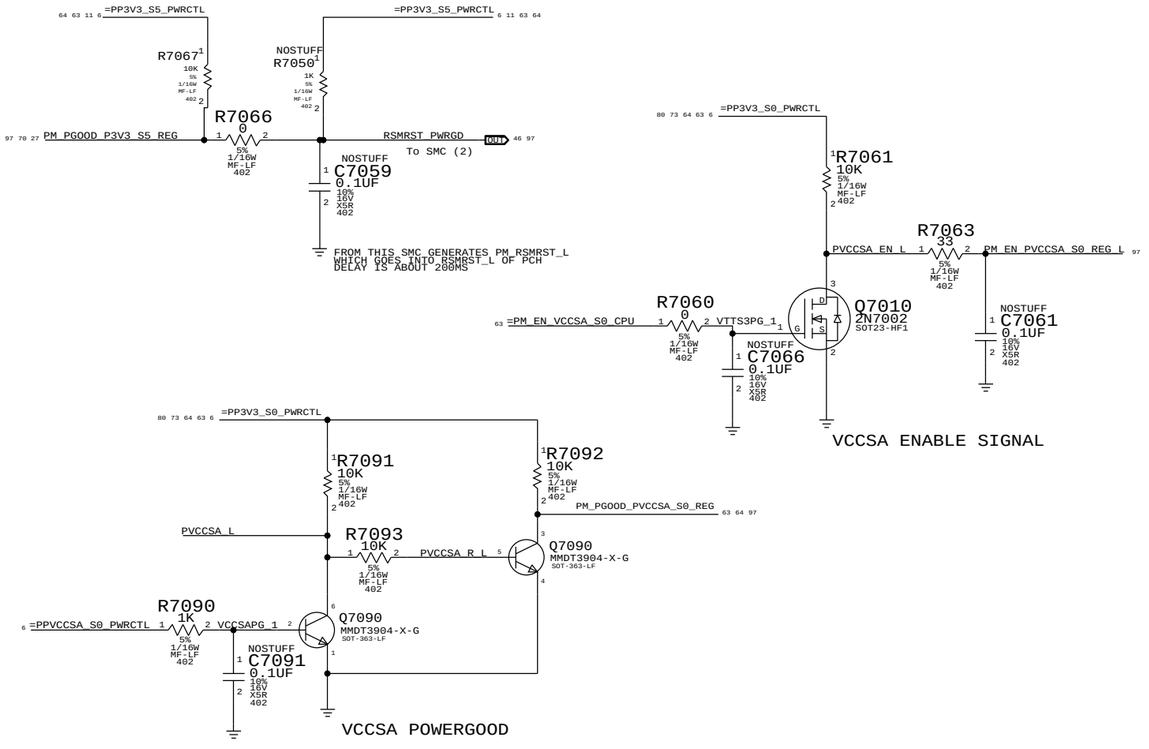
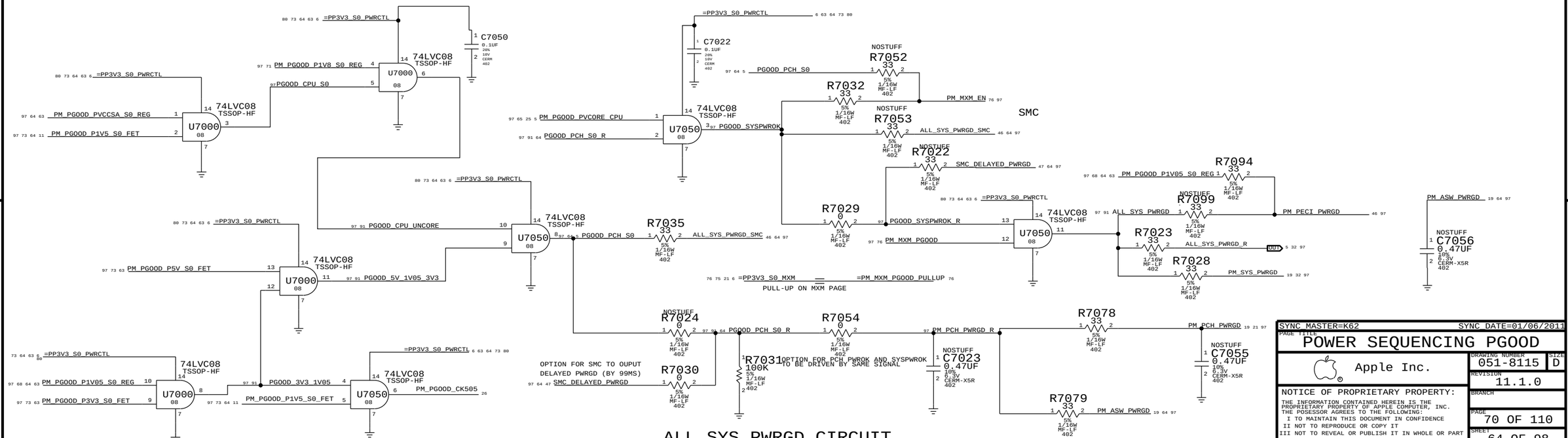
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



S0 RAILS PGOOD





ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
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CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

=PPVAXG_S0_CPU
OMIT XW7120
R7160 1K 5% 1/16W MF-LF 402
R7161 0 5% 1/16W MF-LF 402
R7162 10 5% 1/16W MF-LF 402
VR_AXG_VSNS_XW_P
VOLTAGE=1.1V
NET_PHYSICAL_TYPE=SNS_DIFF
VR_AXG_VSNS_R_P
VR_AXG_VSEN
SIGNAL_MODEL=EMPTY
CPU_VAXG_SENSE_P
CPU_VAXG_SENSE_N
1.25 mOhm loadline
R7163 0 5% 1/10W MF-LF 402
R7164 10 5% 1/16W MF-LF 402
VR_AXG_VSNS_R_N
VR_AXG_RGND
NOSTUFF C7155 0.0022UF 10% 50V CERM 402
XW7130 SM OMIT
R7165 1K 5% 1/16W MF-LF 402
VR_AXG_VSNS_XW_N
VOLTAGE=0V
NET_PHYSICAL_TYPE=SNS_DIFF
C7156 0.0022UF 10% 50V CERM 402
C7157 0.0022UF 10% 50V CERM 402
AGND_CPU

=PP5V_S0_VRD
R7127 2.2 5% 1/8W MF-LF 805
PP5V_S0_CPU_VCORE_VCC
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V

=PP3V3_S0_VRD
R7157 1K 5% 1/10W MF-LF 402
C7114 10UF 20% 6.3V X5R 805
AGND_CPU
R7103 0603 6.8K
C7113 0.1UF 10% 10V X5R 402
VR_AXG_TM
LOCAL 5V
U7100 ISL6364 QFN
VCC
NO_VAXG R7100 0 5% 1/16W MF-LF 402
NOSTUFF R7101 0 5% 1/16W MF-LF 402
NOSTUFF R7102 0 5% 1/16W MF-LF 402
NOSTUFF R7103 0 5% 1/16W MF-LF 402
NOSTUFF R7104 0 5% 1/16W MF-LF 402
NOSTUFF R7105 0 5% 1/16W MF-LF 402
R7106 0 5% 1/16W MF-LF 402
VAXG R7107 0 5% 1/16W MF-LF 402
VR_AXG_PWM
R7189 1K 5% 1/16W MF-LF 402
NOSTUFF C7115 0.01UF 10% 16V CERM 402
AGND_CPU
R7141 1.21K 1% 1/16W MF-LF 402
VR_AXG_HFREQ_COMP
VR_AXG_FB
VR_AXG_COMP
PM_PGOOD_PVCORE_CPU
R7195 10K 5% 1/16W MF-LF 402
VR_AXG_SW_FREQ
VR_AXG_IMON
VR_CPU_SW_FREQ
VR_CPU_RAMP_ADJ
PM_EN_PVCORE_CPU
VR_EN_PWR_OVP
VR_AXG_PWM_R
VR_AXG_ISNS_R_P
VR_AXG_ISNS_R_N
VR_CPU_PWM1_R
VR_CPU_ISNS1_R_N
VR_CPU_PWM2_R
VR_CPU_ISNS2_R_N
VR_CPU_PWM3_R
VR_CPU_ISNS3_R_N
VR_CPU_PWM4_R
TMS
VSENS
HFCOMPS/DVCS
FBS
RGNDS
COMPS
VR_RDY
BTS_DES_TCOMPS
BT_FDVID_TCOMP
NPSI_DE_IMAX
ADDR_IMAXS_TMAX
SVCLK
SVALERT*
SVDATA
VSEN
RGND
FB
PSICOMP
HFCOMP
COMP
SICI
IMON
VR_HOT*
TM
PWMS
ISNS+
ISNS-
PWM1
ISEN1+
ISEN1-
PWM2
ISEN2+
ISEN2-
PWM3
ISEN3+
ISEN3-
PWM4
ISEN4+
ISEN4-
FSS_DRPS
VR_RDYS
IMONS
FS_DRP
RAMP_ADJ
EN_VTT
EN_PWR
RSET
THRM PAD 49

CPU VCORE
VOUT = VCORE
PEAK = 75A
AVG = 55A

VAXG R7108 110 1% 1/16W MF-LF 402
VAXG C7100 220PF 10% 50V X7R-CERM 402
VAXG C7101 0.1UF 10% 10V X5R 402
VAXG C7102 220PF 10% 50V X7R-CERM 402
AGND_CPU
VAXG R7109 1.02K 1% 1/16W MF-LF 402
DIFFERENTIAL_PAIR=VR_AXG_ISNS
VR_AXG_ISNS_P
VR_AXG_ISNS_N
R7110 0 1/16W 5% MF-LF 402
VR_CPU_PWM1
C7103 220PF 10% 50V X7R-CERM 402
C7104 0.1UF 10% 10V X5R 402
R7111 1.02K 1% 1/16W MF-LF 402
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
DIFFERENTIAL_PAIR=VR_CPU_ISNS1
R7112 0 1/16W 5% MF-LF 402
VR_CPU_PWM2
C7105 220PF 10% 50V X7R-CERM 402
C7106 0.1UF 10% 16V X5R 402
R7113 1.02K 1% 1/16W MF-LF 402
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
DIFFERENTIAL_PAIR=VR_CPU_ISNS2
R7114 0 1/16W 5% MF-LF 402
VR_CPU_PWM3
C7107 220PF 10% 50V X7R-CERM 402
C7108 0.1UF 10% 16V X5R 402
R7115 1.02K 1% 1/16W MF-LF 402
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
DIFFERENTIAL_PAIR=VR_CPU_ISNS3

C7116 0.001UF 10% 50V CERM 402
R7128 249 1% 1/16W MF-LF 402
VR_SEN_R2
R7129 499 1% 1/16W MF-LF 402
R7130 309 1% 1/16W MF-LF 402
VR_SEN_R3
R7131 10 5% 1/16W MF-LF 402
VR_SEN_R1
R7132 9.09K 1% 1/16W MF-LF 402
VR_AXG_COMP_RC
C7117 3900PF 10% 50V X7R 0402
C7118 39PF 5% 50V CERM 402

C7119 4700PF 10% 100V CERM 402
VR_CPU_PSICOMP2
VR_CPU_PSICOMP1
R7133 402 1% 1/16W MF-LF 402
R7134 249 1% 1/16W MF-LF 402
VR_CPU_FB_RC
C7120 390PF 10% 50V CERM 402
R7135 1.3K 1% 1/16W MF-LF 402
VR_CPU_FB_R
R7136 215 1% 1/16W MF-LF 402
R7121 10 5% 1/16W MF-LF 402
C7122 82PF 5% 50V CERM 402
R7145 4.99K 1% 1/16W MF-LF 402
VR_CPU_FB2
C7123 0.0012UF 10% 50V CERM 402

PP5V_S0_CPU_VCORE_VCC
R7156 953K 1% 1/16W MF-LF 402
R7140 953K 1% 1/16W MF-LF 402
R7142 23.2K 1% 1/16W MF-LF 402
R7143 15.0K 1% 1/16W MF-LF 402
CPU_VIDSCLK
CPU_VIDALERT_L
CPU_VIDSOUT
VR_CPU_FB
VR_CPU_PSICOMP
R7144 2.32K 1% 1/16W MF-LF 402
VR_CPU_HFREQ_COMP
VR_CPU_COMP
VR_CPU_IALUTO
VR_CPU_IMON
VR_CPU_VSEN
SIGNAL_MODEL=EMPTY
NOSTUFF C7158 0.0022UF 10% 50V CERM 402
1.25 mOhm loadline
CPU_VCC_SENSE_P
CPU_VCC_SENSE_N
R7169 0 5% 1/16W MF-LF 402
R7170 10 5% 1/16W MF-LF 402
VR_CPU_VSNS_R_N
VR_CPU_RGND
XW7133 SM OMIT
R7171 1K 5% 1/16W MF-LF 402
VR_CPU_VSNS_XW_N
VOLTAGE=0V
NET_PHYSICAL_TYPE=SNS_DIFF
C7159 0.0022UF 10% 50V CERM 402
C7160 0.0022UF 10% 50V CERM 402
AGND_CPU

CPU_PROCHOT_L
R7199 0 5% 1/16W MF-LF 402
VR_HOT_L
VR_CPU_TM
R7149 30.1K 1% 1/16W MF-LF 402
R7150 17.8K 1% 1/16W MF-LF 402
R7151 255K 1% 1/16W MF-LF 402
R7158 255K 1% 1/16W MF-LF 402
R7146 110 5% 1/10W MF-LF 402
NOSTUFF R7147 90.9 1% 1/10W MF-LF 402
R7148 54.9 1% 1/10W MF-LF 402
C7126 0.1UF 10% 16V X5R 402
R7152 0 5% 1/10W MF-LF 402
C7124 0.01UF 10% 16V CERM 402
AGND_CPU
=PPVCCIO_S0_CPU
R7159 1K 5% 1/16W MF-LF 402
RT7104 0603 6.8K
C7132 0.1UF 10% 10V X5R 402
PP5V_S0_CPU_VCORE_VCC
NOSTUFF R7179 100K 5% 1/16W MF-LF 402
AGND_CPU
R7153 0 5% 1/16W MF-LF 402
VR_CPU_IMON_R
C7127 27.0NF 10% 16V X5R 402
R7154 11K 1% 1/16W MF-LF 402
AGND_CPU
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0V
OMIT XW7101 SM
R7120 124K 1% 1/16W MF-LF 402
VR_RSET
R7119 11K 1% 1/16W MF-LF 402
R7155 105K 1% 1/16W MF-LF 402
R7122 100K 5% 1/16W MF-LF 402
R7123 2.74K 1% 1/16W MF-LF 402
VR_EN_PWR_OVP_R
R7124 6.65K 1% 1/16W MF-LF 402
AGND_CPU
R7118 1.18M 1% 1/16W MF 402
PP12V_S0_CPU_FLTRD
C7112 0.1UF 10% 16V X5R 402
NOSTUFF R7181 10K 1% 1/16W MF-LF 402
AGND_CPU
NOSTUFF R7180 100K 5% 1/16W MF-LF 402
PP5V_S0_CPU_VCORE_VCC
R7125 1K 1% 1/16W MF-LF 402
VR_AXG_IMON_R
C7111 0.1UF 10% 16V X5R 402
R7126 13.7K 1% 1/16W MF-LF 402
AGND_CPU

=PPVCORE_S0_CPU
OMIT XW7123
R7166 1K 5% 1/16W MF-LF 402
R7167 10 5% 1/16W MF-LF 402
R7168 0 5% 1/16W MF-LF 402
VR_CPU_VSNS_XW_P
VOLTAGE=1.1V
NET_PHYSICAL_TYPE=SNS_DIFF
VR_CPU_VSNS_R_P
VR_CPU_VSEN
SIGNAL_MODEL=EMPTY
CPU_VCC_SENSE_P
CPU_VCC_SENSE_N
1.25 mOhm loadline
R7169 0 5% 1/16W MF-LF 402
R7170 10 5% 1/16W MF-LF 402
VR_CPU_VSNS_R_N
VR_CPU_RGND
XW7133 SM OMIT
R7171 1K 5% 1/16W MF-LF 402
VR_CPU_VSNS_XW_N
VOLTAGE=0V
NET_PHYSICAL_TYPE=SNS_DIFF
C7159 0.0022UF 10% 50V CERM 402
C7160 0.0022UF 10% 50V CERM 402
AGND_CPU

=PP12V_S0_VRD
L7100 1UH-20A-4.5MOHM TH-VERT-HF
PP12V_S0_CPU_FLTRD
NET_PHYSICAL_TYPE=POWER
VOLTAGE=12V
CPU CORE INPUT FILTER

SYNC_MASTER=K60_AARON SYNC_DATE=N/A
PAGE TITLE
VREG: PPVCORE_S0_CPU
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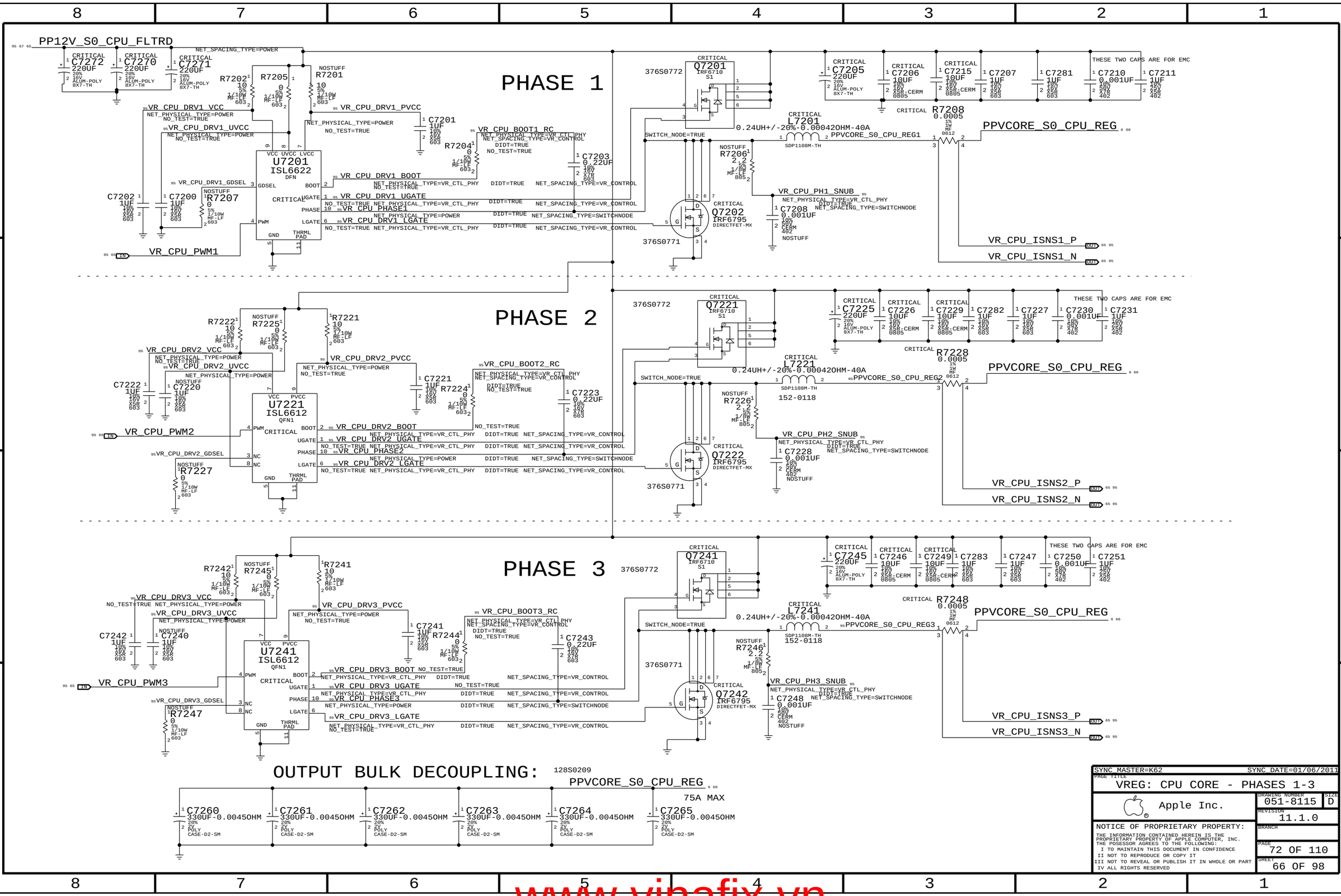
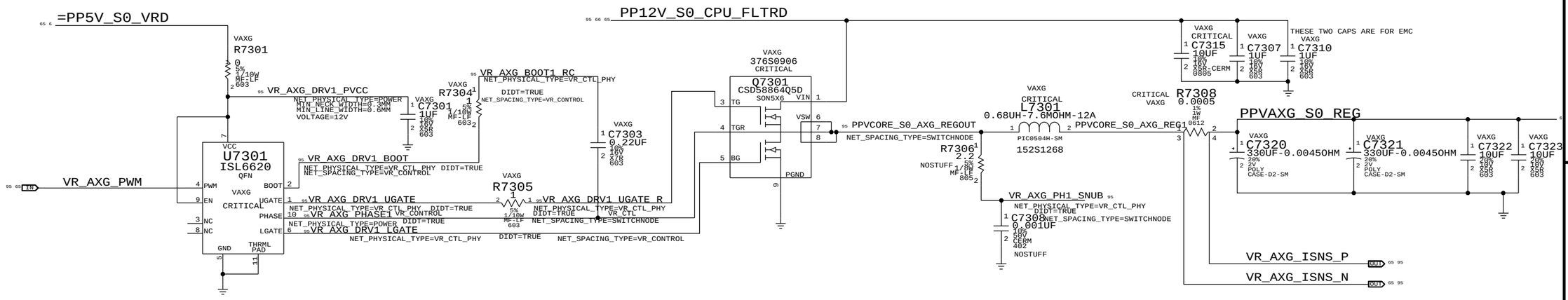


AXG PHASE (MAX 15A)



SYNC_MASTER=K60_AARON	SYNC_DATE=N/A
PAGE TITLE: VREG:AXG PHASE/CORE - CAPS	
Apple Inc.	DRAWING NUMBER: 051-8115 · SIZE: D
	REVISION: 11.1.0
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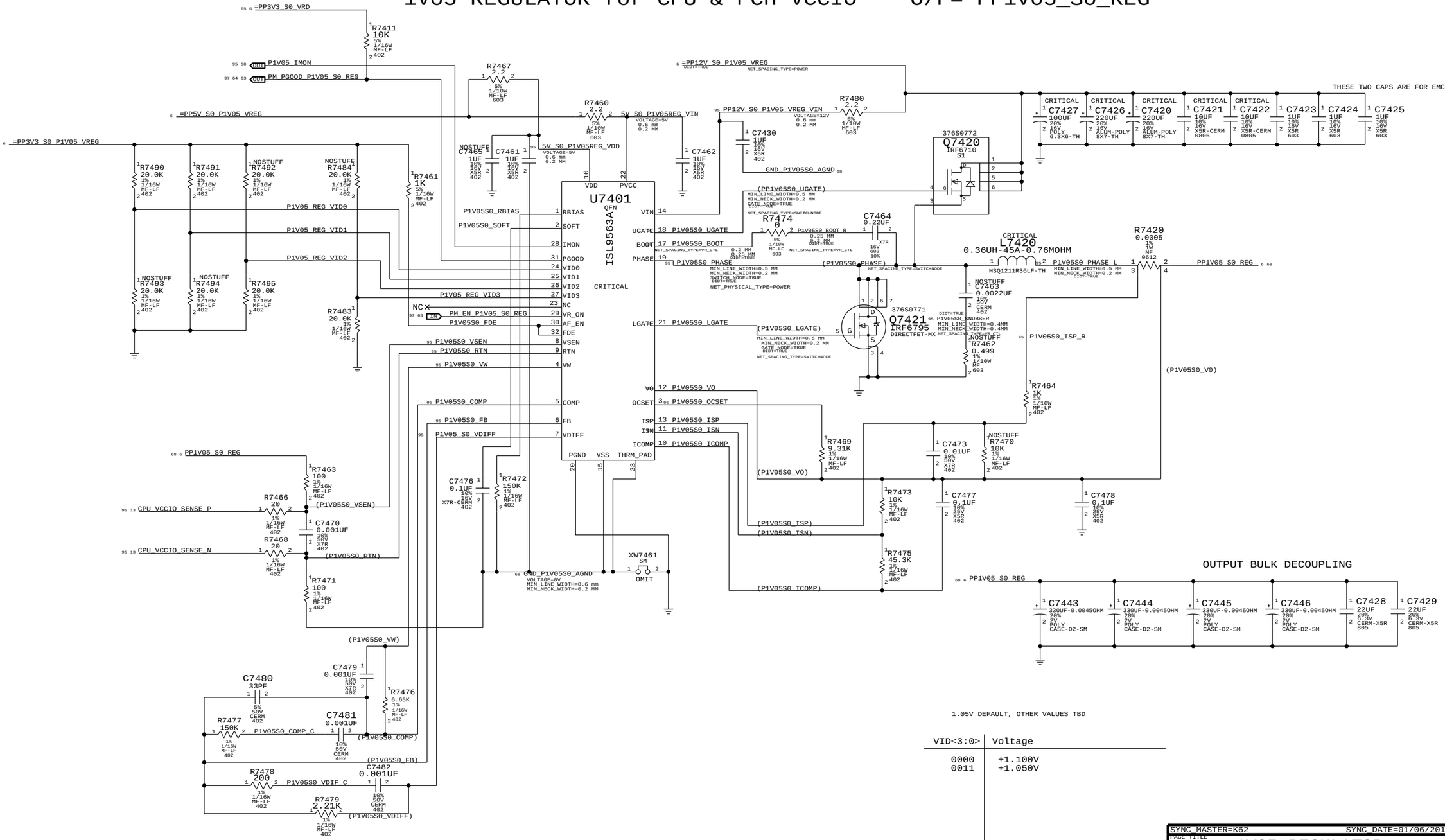
1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1V05 REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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CPU VCCSA 0.925V (8.8A MAX)

=PP3V3_S5_CPU_VCCSA

R7531 100 5% 1/10W MF-LF 402

VCCSA_REF

CRITICAL
U7505 ISL21070 SOT23-3
VIN VOUT GND

C7515 1UF 10% 10V X5R 402

C7516 1UF 10% 10V X5R 402

C7551 10PF 5% 50V CERM 402

R7550 49.9K 1% 1/16W MF-LF 402

VCCSA_FIL

C7550 560PF 10% 50V CERM 402

=PPVCCIO_S0_CPU_VCCSA

NOTE: THIS RAIL IS COMING FROM PPVCCSA_S0_INPUT_SNS AFTER SENSE RES

R7505 0 5% 1/10W MF-LF 402

VCCSA_GATE
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

Q7500 IRFH3702TRPBF PQFN
376S0910

VCCSA_CNTRL_INPUT1

LM358-SOI-HF U7501

VCCSA_OUT
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

NOSTUFF
R7506 1K 5% 1/10W MF-LF 402
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
NET_SPACING_TYPE=POWER

PPVCCSA_S0_FET

OMIT_TABLE
C7509 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM

OMIT_TABLE
C7510 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM

C7507 10UF 10% 6.3V X5R 805

C7508 10UF 10% 6.3V X5R 805

Place C7507 inside cavity
Place C7508 inside cavity

=PP12V_S0_CPU_VCCSA

R7504 2.2 5% 1/10W MF-LF 603

VCCSA_PWR_RC

C7502 1UF 10% 25V X5R 603-1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

VCCSA_CNTRL_INPUT2

R7507 5.49K 1% 1/16W MF-LF 402

VCCSA_CNTRL_INPUT2_R

R7535 22 5% 1/10W MF-LF 402

R7533 10K 1% 1/16W MF-LF 402

NOSTUFF
C7512 10PF 5% 50V CERM 402

R7552 1K 5% 1/16W MF-LF 402

VCCSA_CRL

C7552 1000PF 5% 25V NP0-C0G 402

CPU_VCCSA_SENSE

R7503 0 5% 1/10W MF-LF 402

C7501 100PF 5% 50V CERM 402

=PPVCCSA_S0_INPUT_PWR

CRITICAL
C7506 330UF-0.009OHM 20% 2V POLY CASE-D2-HF

C7504 4.7UF 20% 6.3V X5R-CERM1 402

C7505 0.1UF 20% 10V CERM 402

LM358-SOI-HF U7501

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

SYNC_MASTER=K62 SYNC_DATE=11/15/2010

PAGE TITLE
CPU VCCSA REGULATOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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SHEET 69 OF 98

3V3 S5 REGULATOR

3V3 OUTPUT

=PP12V_S5_P5VS3_VREG
NET_SPACING_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
DIDT=TRUE

PP3V3_S5_REG
R7776 0.002 1% 1/4W MF-LF 1206
CRITICAL
L7710 2.2UH-14A MMD06CZ-SM
PP3V3_S5_REG_R
NET_PHYSICAL_TYPE=POWER
C7790 0.01UF 10% 16V CERM 402
R7790 15.8K 1% 1/16W MF-LF 402
R7791 15.8K 1% 1/16W MF-LF 402
C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
NET_SPACING_TYPE=VR_CTL
R7730 0.499 1% 1/10W MF 603
P3V3S5_REG_SNUB
DIDT=TRUE

Q7710
RJK0384DPA
WPAK
376S0801
D1
G1 1 (P3V3S5_UGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL
S1/D2 7
G2 6 (P3V3S5_LGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL
S2

C7714 0.1UF 10% 50V X7R 603-1
P3V3S5_REG_BOOT_R
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
DIDT=TRUE
NET_SPACING_TYPE=VR_CONTROL
(P3V3S5_PHASE)
R7710 0 5% 1/10W MF-LF 603
NET_SPACING_TYPE=VR_CONTROL
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING:
PLACEMENT_NOTE=PLACE NEXT TO C7716
C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
128S0237
CRITICAL
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
XW7716 SM OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>
R7724 976 1% 1/16W MF-LF 402
P3V3S5_REG_FB_R
C7720 1000PF 5% 25V NP0-C0G 402

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603
EMC CAPS
PLACE CLOSE TO L

Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402
R7723 33K 5% 1/16W MF-LF 402

U7700
ISL62383
QFN
CRITICAL

LDO5	18		
VCC1	5		
VCC2	4		
VIN	17	VIN_5V_S5_REG_RC	
FCCM	3	TP_P5VS3_REG_FCCM	
PGOOD1	7	PM_PGOOD_P3V3_S5_REG	
UGATE1	14	P3V3S5_REG_UGATE	
BOOT1	15	P3V3S5_REG_BOOT	
PHASE1	13	P3V3S5_REG_PHASE	
LGATE1	16	P3V3S5_REG_LGATE	
ISEN1	10	P3V3S5_REG_ISEN	
OCSET1	11	P3V3S5_REG_OCSET	
VOUT1	9	P3V3S5_REG_VOUT1	
FB1	8	P3V3S5_REG_FB	
FSET1	6	P3V3S5_REG_FSET1	
EN1	12		
PGOOD2	1		
UGATE2	22	P5VS3_REG_UGATE	
BOOT2	21	P5VS3_REG_BOOT	
PHASE2	23	P5VS3_REG_PHASE	
LGATE2	20	P5VS3_REG_LGATE	
ISEN2	26	P5VS3_REG_ISEN	
OCSET2	25	P5VS3_REG_OCSET	
VOUT2	27	P5VS3_REG_VOUT2	
FB2	28	P5VS3_REG_FB	
FSET2	2	P5VS3_REG_FSET2	
EN2	24		
THRM PAD	29	PGND	29

PM_EN_P3V3_S5_REG
PM_EN_P5V_S3_REG

C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402
C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402
NOSTUFF
C7777 0.001UF 10% 50V CERM 402

5V S3 REGULATOR

Power Rating ?

C7719 100UF 20% 16V POLY 6.3X6-TH
C7766 100UF 20% 16V POLY 6.3X6-TH
C7767 100UF 20% 16V POLY 6.3X6-TH
C7768 100UF 20% 16V POLY 6.3X6-TH
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

=PP3V3_S5_VRD
R7726 20K 5% 1/16W MF-LF 402

=PP12V_S5_P5VS3_VREG
NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO
EMC: C7753-C7755
PLACE AT Q7330
C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
R7741 1 5% 1/8W MF-LF 805
P5V_S5_LDO_R
P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

PM_PGOOD_P5V_S3_REG
CRITICAL
Q7750 FDMS0346 POWER56 376S0875
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=VR_CONTROL

R7750 0 5% 1/10W MF-LF 603
P5VS3_REG_BOOT_R
C7756 0.1UF 10% 25V X5R 402
NET_SPACING_TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER
NOSTUFF
C7757 0.001UF 10% 50V CERM 402
5V_SNUBBER
R7752 0.499 1% 1/10W MF 603 NOSTUFF
CRITICAL
Q7751 FDMS0355S POWER56 376S0917

5V OUTPUT

EMC: C7763-C7764
PLACE AT L7750.2
C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG
R7775 0.002 1% 1/4W MF-LF 1206
CRITICAL
L7750 2.2UH+/-20%-0.0069OHM-16A PIC1005H-SM
PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER
R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 10V X5R 402
R7771 9.76K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:
C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1
CRITICAL
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
XW7751 SM OMIT

R7759 976 1% 1/16W MF-LF 402
P5V5_REG_FB_R
C7759 1000PF 5% 25V NP0-C0G 402
R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF-LF 402 RB

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8115
	SIZE D
	REVISION 11.1.0
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	PAGE 77 OF 110
	SHEET 70 OF 98

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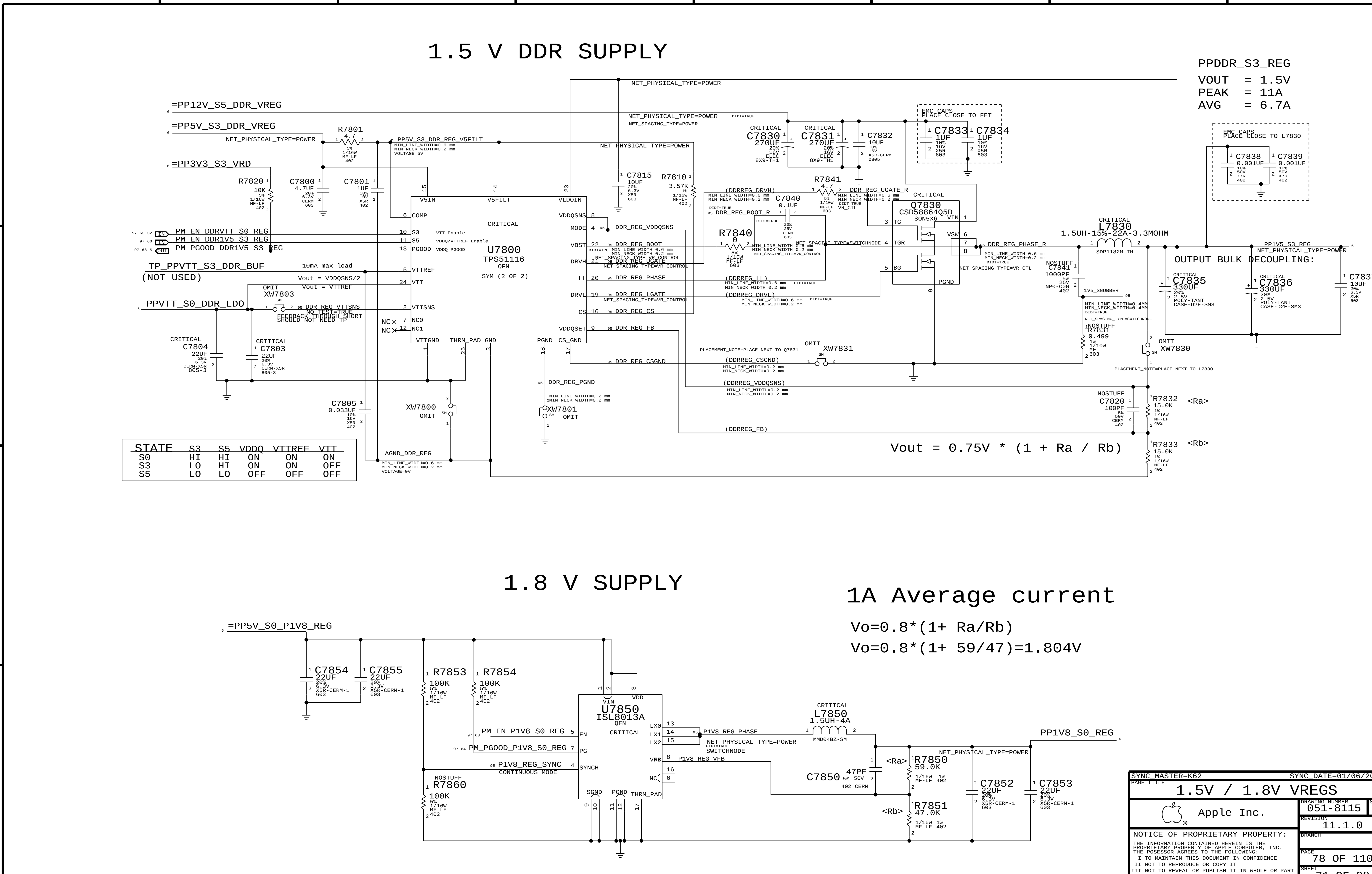

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1.5V / 1.8V VREGS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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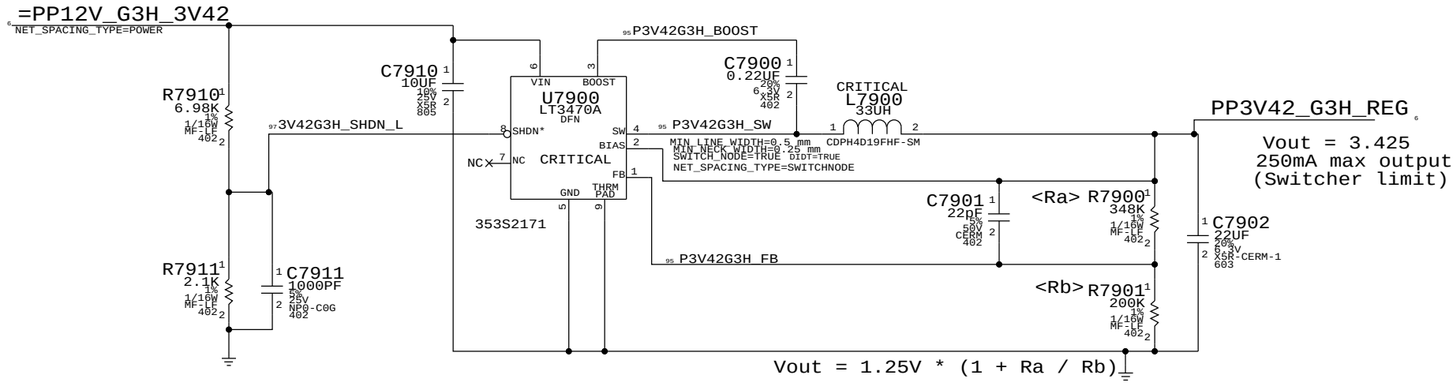
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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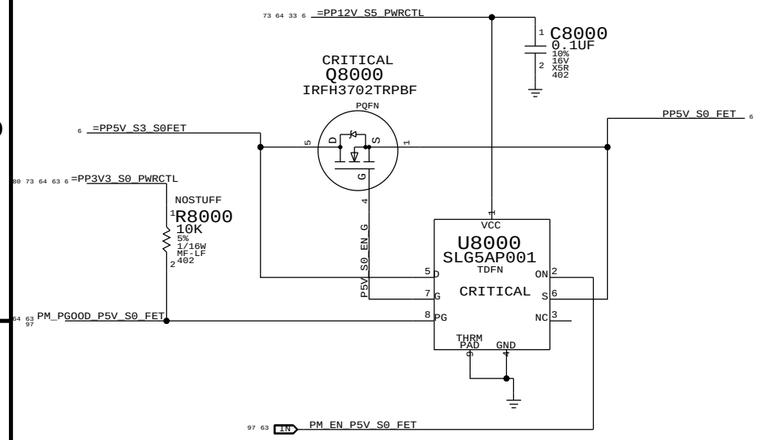
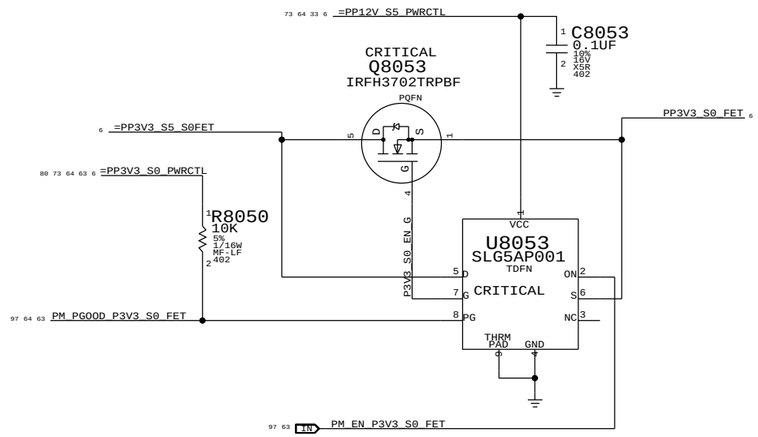
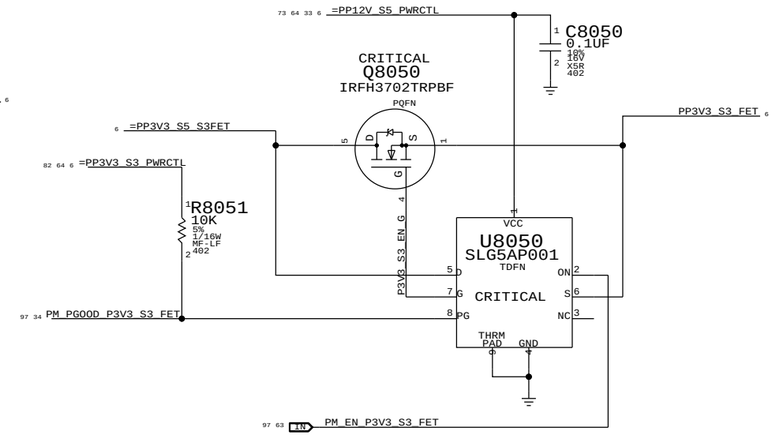
5V S0 FET (6.6A PK/3.1A AVG)



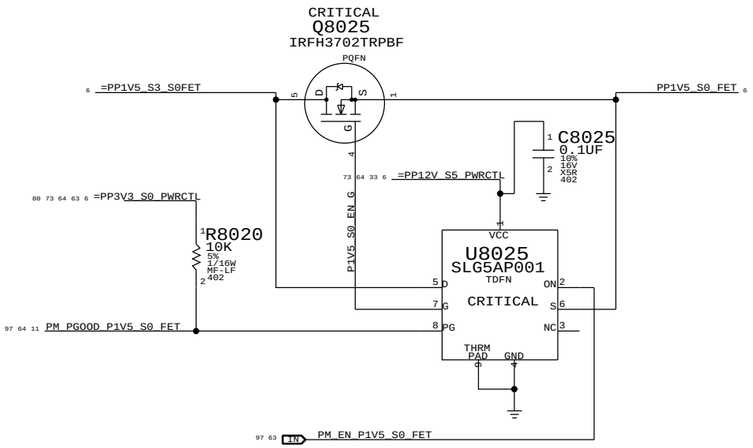
3.3V S0 FET (2.9APK / 2.0A AVG)



3.3V S3 FET (3.4A PK / 1.6A AVG)



1.5V S0 FET (4.8A PK / 4.8A AVG)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: S3+S0 FETS

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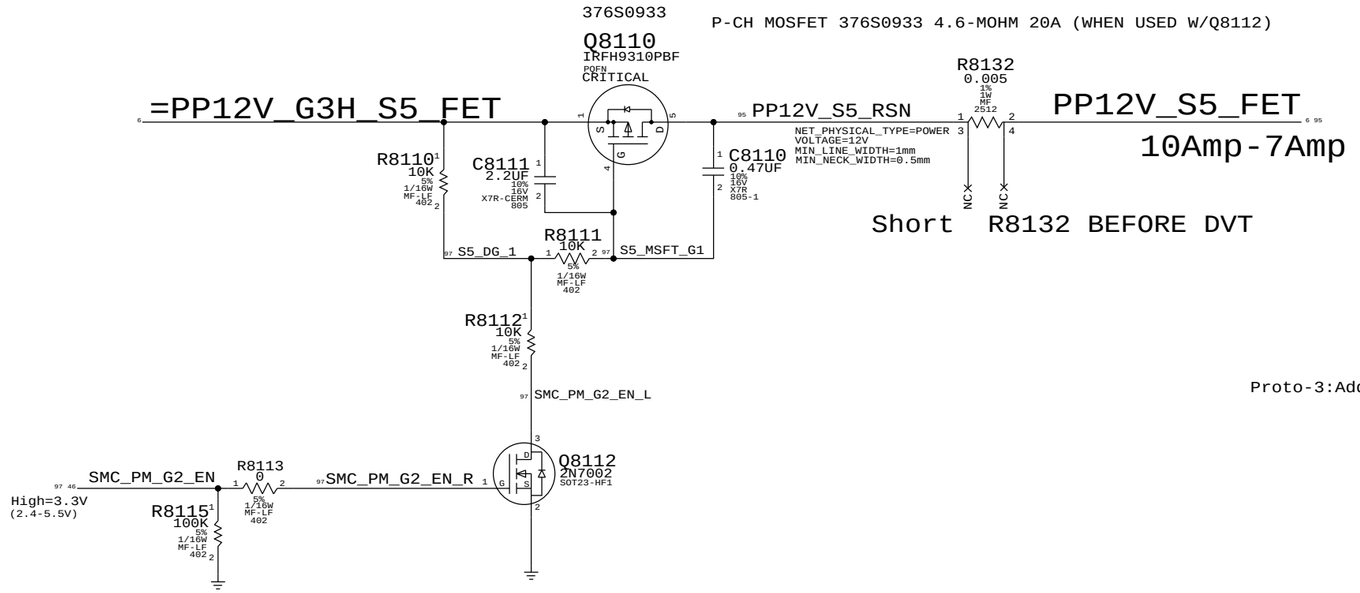

SYNC_MASTER=K60 JERRY SYNC_DATE=01/06/2011

PAGE TITLE
12V_S0 & 12V_S5 switch

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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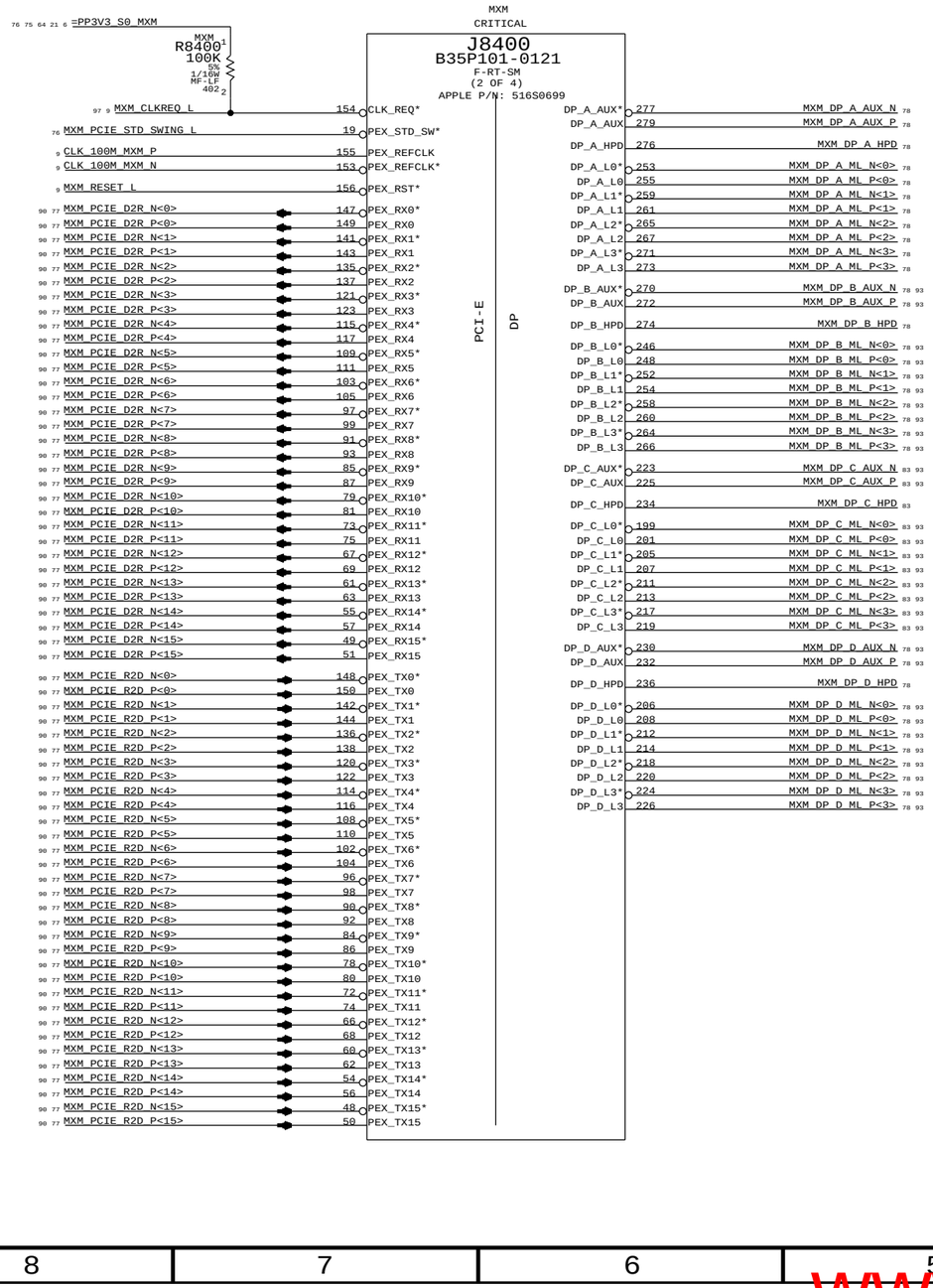
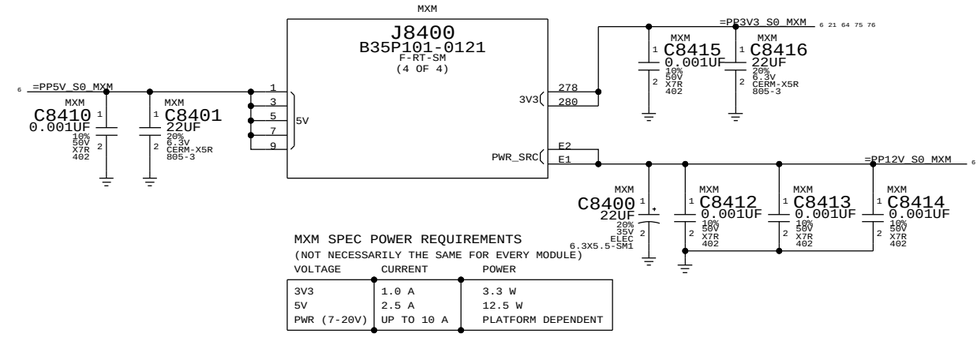
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
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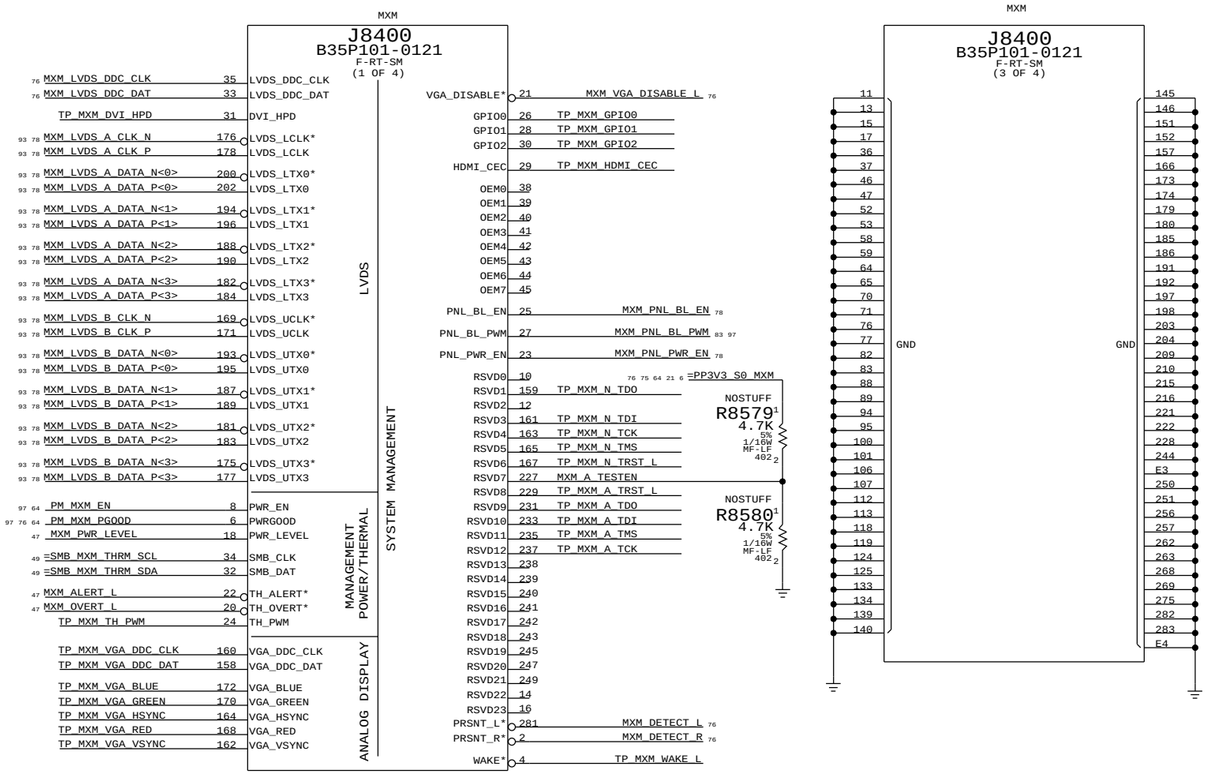
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



ELOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

ELOAT = LOW SWING
GND = HIGH SWING

NOSTUFF R8510 0 MF-LF 5% 1/16W 402
MXM R8504 0 MF-LF 5% 1/16W 402
MXM_VGA_DISABLE_L
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM

R8500 100K MF-LF 5% 1/16W 402 — MXM_DETECT_L

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501 100K MF-LF 5% 1/16W 402 — MXM_DETECT_R

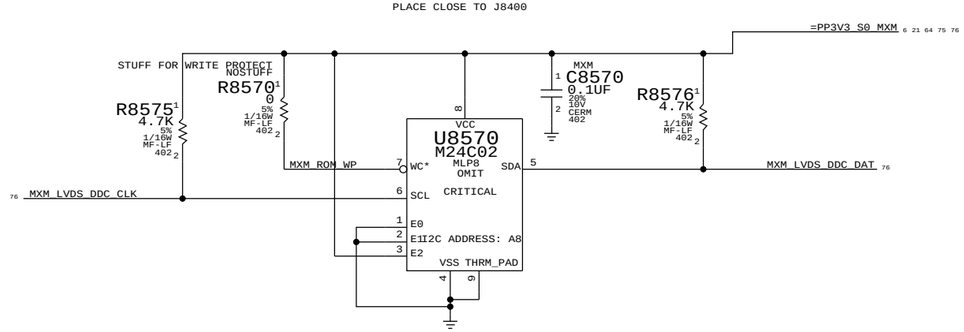
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K MF-LF 5% 1/16W 402 — PM_MXM_PGOOD

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC_MASTER=K60_MASTER SYNC_DATE=N/A

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 85 OF 110
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MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>		
PEG_R2D_C_N<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>		
PEG_R2D_C_N<1>	MXM	C8602	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>		
PEG_R2D_C_P<1>	MXM	C8603	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>		
PEG_R2D_C_N<2>	MXM	C8604	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>		
PEG_R2D_C_P<2>	MXM	C8605	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>		
PEG_R2D_C_P<3>	MXM	C8606	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>		
PEG_R2D_C_N<3>	MXM	C8607	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>		
PEG_R2D_C_N<4>	MXM	C8608	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>		
PEG_R2D_C_P<4>	MXM	C8609	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>		
PEG_R2D_C_N<5>	MXM	C8610	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>		
PEG_R2D_C_P<5>	MXM	C8611	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>		
PEG_R2D_C_P<6>	MXM	C8612	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>		
PEG_R2D_C_N<6>	MXM	C8613	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>		
PEG_R2D_C_N<7>	MXM	C8614	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>		
PEG_R2D_C_P<7>	MXM	C8615	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>		
PEG_R2D_C_P<8>	MXM	C8616	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>		
PEG_R2D_C_N<8>	MXM	C8617	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>		
PEG_R2D_C_P<9>	MXM	C8618	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>		
PEG_R2D_C_N<9>	MXM	C8619	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>		
PEG_R2D_C_N<10>	MXM	C8620	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>		
PEG_R2D_C_P<10>	MXM	C8621	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>		
PEG_R2D_C_N<11>	MXM	C8622	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>		
PEG_R2D_C_P<11>	MXM	C8623	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>		
PEG_R2D_C_P<12>	MXM	C8624	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>		
PEG_R2D_C_N<12>	MXM	C8625	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>		
PEG_R2D_C_N<13>	MXM	C8626	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>		
PEG_R2D_C_P<13>	MXM	C8627	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>		
PEG_R2D_C_P<14>	MXM	C8628	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>		
PEG_R2D_C_N<14>	MXM	C8629	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>		
PEG_R2D_C_N<15>	MXM	C8630	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>		
PEG_R2D_C_P<15>	MXM	C8631	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>		

MXM RX CAPS

MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>		
MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>		
MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>		
MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>		
MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<2>		
MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>		
MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<3>		
MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>		
MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<4>		
MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<4>		
MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<5>		
MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<5>		
MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<6>		
MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<6>		
MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<7>		
MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<7>		
MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<8>		
MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<8>		
MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<9>		
MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<9>		
MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<10>		
MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<10>		
MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>		
MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>		
MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<12>		
MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<12>		
MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<13>		
MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<13>		
MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<14>		
MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>		
MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>		
MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>		

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

75	MXM_DP_A_ML_P<0..3>	==	DP_EXTA_ML_C_P<0..3>	84 93	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_A_ML_N<0..3>	==	DP_EXTA_ML_C_N<0..3>	84 93	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_A_AUX_P	==	DP_EXTA_AUXCH_C_P	78 84 93	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_A_AUX_N	==	DP_EXTA_AUXCH_C_N	78 84 93	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_A_HPD	==	DP_EXTA_HPD	84	MAKE_BASE=TRUE NO_TEST=TRUE

T29 CONN POWER CONTROL ALIAS

95 84	PP3V3_SW_DPAPWR	==	=PP3V3_SW_DPAPWR	6
97 36 33 19	PCIE_WAKE_L	==	=T29_WAKE_L	84

Unused MXM Interfaces

93 76	MXM_LVDS_A_CLK_N	==	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_CLK_P	==	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_N<3..0>	==	NC_MXM_LVDS_A_DATA_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_P<3..0>	==	NC_MXM_LVDS_A_DATA_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_N	==	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_P	==	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_N<3..0>	==	NC_MXM_LVDS_B_DATA_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_P<3..0>	==	NC_MXM_LVDS_B_DATA_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

T29 MXM DP ALIAS

93 75	MXM_DP_D_ML_P<0..3>	==	DP_T29SNK0_ML_C_P<0..3>	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_D_ML_N<0..3>	==	DP_T29SNK0_ML_C_N<0..3>	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_D_AUX_P	==	DP_T29SNK0_AUXCH_C_P	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_D_AUX_N	==	DP_T29SNK0_AUXCH_C_N	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_D_HPD	==	DP_T29SNK0_HPD	86	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_B_ML_P<0..3>	==	DP_T29SNK1_ML_C_P<0..3>	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_B_ML_N<0..3>	==	DP_T29SNK1_ML_C_N<0..3>	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_B_AUX_P	==	DP_T29SNK1_AUXCH_C_P	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
93 75	MXM_DP_B_AUX_N	==	DP_T29SNK1_AUXCH_C_N	86 96	MAKE_BASE=TRUE NO_TEST=TRUE
75	MXM_DP_B_HPD	==	DP_T29SNK1_HPD	86	MAKE_BASE=TRUE NO_TEST=TRUE

Unused T29 Interfaces

96 86	T29_D2R_N<2..3>	==	NC_T29_D2R_N<2..3>				MAKE_BASE=TRUE NO_TEST=TRUE
96 86	T29_D2R_P<2..3>	==	NC_T29_D2R_P<2..3>				MAKE_BASE=TRUE NO_TEST=TRUE
96 86	T29_R2D_C_N<2..3>	==	NC_T29_R2D_C_N<2..3>				MAKE_BASE=TRUE NO_TEST=TRUE
96 86	T29_R2D_C_P<2..3>	==	NC_T29_R2D_C_P<2..3>				MAKE_BASE=TRUE NO_TEST=TRUE
86	T29_LSEO<3>	==	T29_LSEO_LSOE3	==	T29_LSOE<3>	86	MAKE_BASE=TRUE NO_TEST=TRUE
86	T29_LSEO<2>	==	T29_LSEO_LSEO2	==	T29_LSOE<2>	86	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED MXM CONTROL SIGNALS

76	MXM_PNL_BL_EN	==	NC_MXM_PNL_BL_EN	MAKE_BASE=TRUE NO_TEST=TRUE
76	MXM_PNL_PWR_EN	==	NC_MXM_PNL_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

DDC/AUX ALIAS

93 84 78	DP_EXTA_AUXCH_C_P	==	DP_EXTA_DDC_CLK	84	MAKE_BASE=TRUE
93 84 78	DP_EXTA_AUXCH_C_N	==	DP_EXTA_DDC_DATA	84	MAKE_BASE=TRUE

SYNC_MASTER=K60_AARON SYNC_DATE=07/18/2010

PAGE TITLE
DP ALIAS AND CONTROL

Apple Inc.

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System RTC Power Source & 32kHz / 25MHz Clock Generator

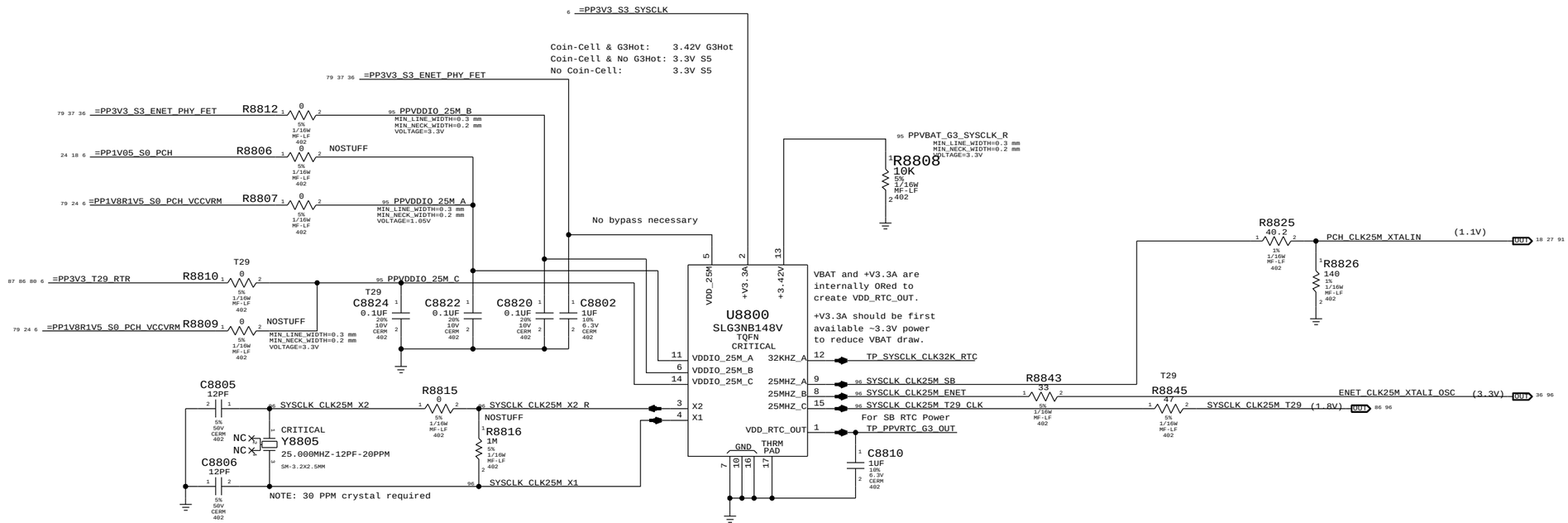
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary



SYNC MASTER=K62	SYNC DATE=01/06/2012
PAGE TITLE	GREEN CLOCK
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
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Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)

Supervisor & CLKREQ# Isolation

T29 CLKREQ# ISOLATION

3.3V T29 Switch

1.05V T29 Switch

U8910	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: T29 POWER

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

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Page Notes

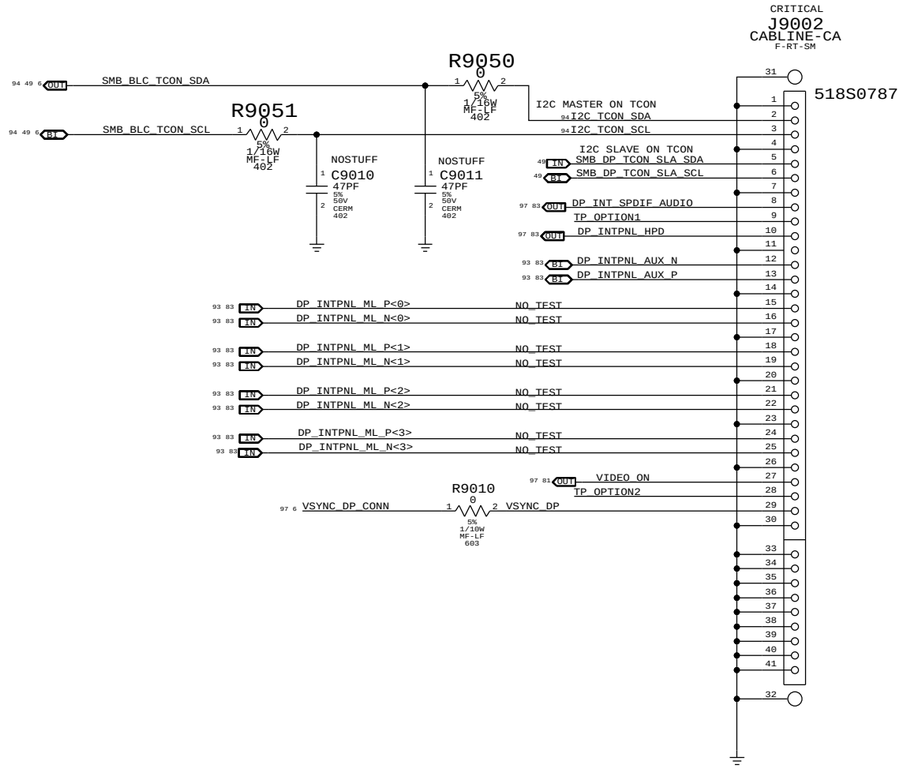
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

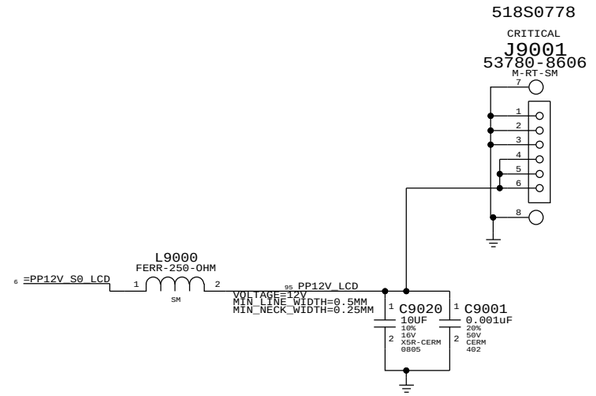
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

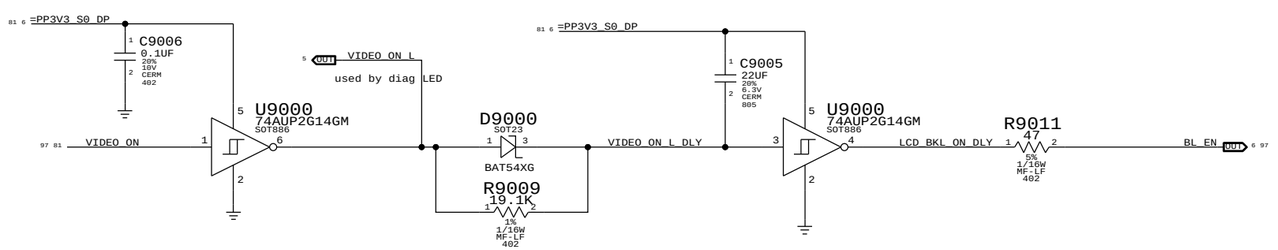


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
Display: Int DP Connector

Apple Inc.

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3V3(DP)/2V9(T29) PORTA SUPPLY

12V T29 PORTA SUPPLY

=PP5V_S3_P3V3R2V9_REG_A

C9120 10UF 10% 16V X5R-CERM 0805

CRITICAL
U9101 ISL80101A DFN

T29_DP_PORTA_PWR_EN_REG
3V3R2V9_SS_A

C9121 0.022UF 10% 16V CERM-X5R 402

R9130 25.5K 1/16W 1% MF-LF 402

C9122 10UF 10% 16V X5R-CERM 0805

R9121 20K 1/16W 5% MF-LF 402

C9123 330PF 10% 50V 402 CERM

PP3V3R2V9_DPAPWR_D

D9101 POWERDI-123 DFLS260

NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

3V3R2V9_DPAPWR_ADJ

=PP3V3_S3_P3V3R2V9_REG_A

R9122 100K 1/16W 5% MF-LF 402

R9123 2.05K 1/16W 1% MF-LF 402

PM_PGOOD_P3V3_2V9_A

PP3V3R12V_SW_DPAPWR

NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0.38MM
VOLTAGE=12V
MIN_NECK_WIDTH=0.20 MM

C9124 10UF 10% 16V X5R-CERM 0805

NOSTUFF C9125 10UF 10% 16V X5R-CERM 0805

R9150 2.2K 1/10W 5% MF-LF 603

R9124 11.5K 1/16W 1% MF-LF 402 <RA>

R9125 15.0K 1/16W 1% MF-LF 402 <RB1>

<RB2>

=PP3V3_S5_P3V3R2V9_A

C9150 0.1UF 10% 16V X5R 402

U9120 MC74VHC1G08 SOT23-5-HF

T29_DP_PORTA_PWR_EN
PM_PGOOD_P5V_S3_REG
T29_DP_PORTA_PWR_EN_REG

NO_T29 R9128 0 5% 1/10W MF-LF 402
PM_SLP_S3_L

=PP3V3_S3_PWRCTL

NOSTUFF R9126 10K 5% 1/16W MF-LF 402

DP_A_PWRDWN_FET_R

NOSTUFF Q9120 2N7002DW-X-G SOT-363

NOSTUFF Q9120 2N7002DW-X-G SOT-363

DP_A_PWRDWN_INV

T29_A_BIAS

LO: 3V3 FOR DP
HI: 2V8 FOR T29
2V9 measured at CDR

VO=0.5*(1+ RA/RB)
VO=3.304V

12 VOLTS
12 WATTS MAX PER PORT

=PP12V_S5_T29_A

T29 R9116 15K 5% 1/16W MF-LF 402

T29 D9103 CRITICAL MMBZ5227BLT1H SOT23

NOSTUFF R9117 13K 5% 1/16W MF-LF 402

T29 Q9115 SSM3K15FV SOD-VESM-HF

T29_A_HV_EN

DPAPWRSW_HVEN_L_R

T29 C9110 0.1UF 10% 50V X7R 603-1

T29 CRITICAL U9110 SN1010017 QFN

EN* (IPU-Weak!)
RTRY*
CT
FLT*
ILIM
IFLT
GND
THRM PAD

T29 C9111 0.1UF 10% 50V X7R 603-1

PP3V3R12V_SW_DPAPWR_D
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=12V

T29 D9105 DSN2 NSR20F20NXT5G

PP3V3R12V_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=12V

TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT

T29 R9112 0 5% 1/16W MF-LF 402 <CT>

T29 R9110 100K 1% 1/16W MF-LF 402 <RFLT>

T29 R9111 174K 1% 1/16W MF-LF 402 <RLIM>

NEED TO UPDATE TABLE BELOW LATER

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200K / RFLT = 2A
ILIM = 201K / RLIM = 1.155A.
TFLT = CCT * 38900
TSD = CCT * 100000

SYNC_MASTER=K62 SYNC_DATE=11/14/2010

PAGE TITLE: 2V9/3V3/12V POWER SWITCH

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
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R9223 0 5% 1/16W MF-LF 402
=PP1V5_S0_DP
PP1V5_S0_DP_R
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF C9273 0.1uF 10% 16V X5R 402

=PP3V3_S0_INTDPMUX
C9268 0.1uF
C9269 0.1uF
C9209 1UF

U9200 CBTL06142CEEG TFBGA
VDD CRITICAL

MXM_DP_C_ML_P<0>
MXM_DP_C_ML_N<0>
MXM_DP_C_ML_P<1>
MXM_DP_C_ML_N<1>
MXM_DP_C_ML_P<2>
MXM_DP_C_ML_N<2>
MXM_DP_C_ML_P<3>
MXM_DP_C_ML_N<3>
DIN1_0+ B4
DIN1_0- A4
DIN1_1+ B5
DIN1_1- A5
DIN1_2+ B6
DIN1_2- A6
DIN1_3+ A8
DIN1_3- A9

PP1V5_S0_DP_R
R9240 470K 5% 1/16W MF-LF 402
R9242 470K 5% 1/16W MF-LF 402

MXM_DP_C_AUX_P C9213 0.1uF
MXM_DP_C_AUX_N C9214 0.1uF
MXM_DP_C_AUX_R_P
MXM_DP_C_AUX_R_N
DAUX1+ H9
DAUX1- J9

NC DDC_CLK1 H8
NC DDC_DAT1 J8

MXM_DP_C_HPD
R9228 100K 5% 1/16W MF-LF 402
HPD_1 J2

DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>
DIN2_0+ B8
DIN2_0- B9
DIN2_1+ D8
DIN2_1- D9
DIN2_2+ E8
DIN2_2- E9
DIN2_3+ F8
DIN2_3- F9

PP1V5_S0_DP_R
T29 R9244 470K 5% 1/16W MF-LF 402
T29 R9245 470K 5% 1/16W MF-LF 402

DP_T29SRC_AUXCH_C_P C9211 0.1uF
DP_T29SRC_AUXCH_C_N C9212 0.1uF
DP_T29SRC_AUXCH_R_C_P
DP_T29SRC_AUXCH_R_C_N
DAUX2+ H6
DAUX2- J6

(For each pair)

NC DDC_CLK2 H5
NC DDC_DAT2 J5

=PP3V3_S0_INTDPMUX
R9220 10K 5% 1/16W MF-LF 402
DP_T29SRC_HPD
HPD_2 H3
DP_GPU_T29_SEL
GPU_SEL A1
XSD* B7
DP_INTMUX_XSD

DDC_AUX_SEL C2
TST0 G2
GND B3 C8 G8 H4 H7

R9237 10K 5% 1/16W MF-LF 402

DOUT_0+ B2
DOUT_0- B1
DOUT_1+ D2
DOUT_1- D1
DOUT_2+ E2
DOUT_2- E1
DOUT_3+ F2
DOUT_3- F1
AUX+ H2
AUX- H1

DP_INTCONN_ML_C_P<0>
DP_INTCONN_ML_C_N<0>
DP_INTCONN_ML_C_P<1>
DP_INTCONN_ML_C_N<1>
DP_INTCONN_ML_C_P<2>
DP_INTCONN_ML_C_N<2>
DP_INTCONN_ML_C_P<3>
DP_INTCONN_ML_C_N<3>
DP_INTCONN_AUXCH_C_P
DP_INTCONN_AUXCH_C_N

C9201 0.1uF
C9202 0.1uF
C9203 0.1uF
C9204 0.1uF
C9205 0.1uF
C9206 0.1uF
C9207 0.1uF
C9208 0.1uF
C9210 0.1uF
C9215 0.1uF

DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
DP_INTPNL_ML_P<2>
DP_INTPNL_ML_N<2>
DP_INTPNL_ML_P<3>
DP_INTPNL_ML_N<3>

HPDIN J1 DP_INTPNL_HPD
NOSTUFF R9227 100K 5% 1/16W MF-LF 402

=PP3V3_S0_INTDPMUX
NOSTUFF R9248 470K 5% 1/16W MF-LF 402
R9249 100K 5% 1/16W MF-LF 402
R9250 100K 5% 1/16W MF-LF 402
NOSTUFF R9251 470K 5% 1/16W MF-LF 402
DP_INTPNL_AUX_P
DP_INTPNL_AUX_N

=PP3V3_S0_INTDPMUX
T29 C9272 0.1uF
T29 U9210 74LVC1G157 SOT487
DP_INT_SPDIF_AUDIO
AUD_SPDIF_IN
DP_GPU_T29_SEL
AUD_SPDIF_IN_CODEC
NO_T29 R9225 0 5% 1/16W MF-LF 402

=PP3V3_S0_INTDPMUX
NOSTUFF R9230 10K 5% 1/16W MF-LF 402
=PP3V3_S0_INTDPMUX
T29 C9270 0.1uF
T29 U9220 74LVC1G157 SOT487
BDV_BKL_PWM
MXM_PNL_BL_PWM
DP_GPU_T29_SEL
R9222 47 5% 1/16W MF-LF 402
LCD_BL_PWM
LCD_BL_FILT
L9201 FERR-220-OHM 0402
BL_PWM
NO_T29 R9226 0 5% 1/16W MF-LF 402

PP1V5_S0_DP_R
T29 R9260 470K 5% 1/16W MF-LF 402
T29 R9261 470K 5% 1/16W MF-LF 402
T29 R9262 470K 5% 1/16W MF-LF 402
T29 R9263 470K 5% 1/16W MF-LF 402
T29 R9264 470K 5% 1/16W MF-LF 402
T29 R9265 470K 5% 1/16W MF-LF 402
T29 R9266 470K 5% 1/16W MF-LF 402
T29 R9267 470K 5% 1/16W MF-LF 402

DP_T29SRC_ML_P<0> C9250 0.1uF
DP_T29SRC_ML_N<0> C9251 0.1uF
DP_T29SRC_ML_P<1> C9252 0.1uF
DP_T29SRC_ML_N<1> C9253 0.1uF
DP_T29SRC_ML_P<2> C9254 0.1uF
DP_T29SRC_ML_N<2> C9255 0.1uF
DP_T29SRC_ML_P<3> C9256 0.1uF
DP_T29SRC_ML_N<3> C9257 0.1uF
T29

DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>

SYNC_MASTER=K62_AARON
SYNC_DATE=N/A
PAGE TITLE: Internal DP MUXing
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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

R9309 1M 5% MF-LF 1/16W 402 =PP3V3_S0_DPSDRVA
R9308 1M 5% MF-LF 1/16W 402

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<0> T29_D2R_P<0> (All 4 L's) T29_D2R_C_P<0> T29_D2R_C_N<0>
L9372 1.0NH+/-0.1NH 0201-1 T29
L9373 1.0NH+/-0.1NH 0201-1 T29
OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_F_N<0> T29_R2D_C_F_P<0>
C9372 0.47UF 20% 4V CERM-X5R-1 201 T29
C9373 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9372.2) GND_VOID=TRUE
(C9373.2) GND_VOID=TRUE
T29_A_BIAS_R2D_P0 VOLTAGE=3.3V
GND_VOID=TRUE (C9370/C9371)
C9370 0.47UF 20% 4V CERM-X5R-1 201 T29
C9371 0.47UF 20% 4V CERM-X5R-1 201 T29
R9372 1.5K 5% MF 1/20W 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
R9373 1.5K 5% MF 1/20W 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
T29_R2D_P<0> T29_R2D_N<0>
T29_A_BIAS_R2D_N0 VOLTAGE=3.3V

T29_D2R_N<1> T29_D2R_P<1>
L9382 1.0NH+/-0.1NH 0201-1 T29
L9383 1.0NH+/-0.1NH 0201-1 T29
OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_F_N<1> T29_R2D_C_F_P<1>
C9382 0.47UF 20% 4V CERM-X5R-1 201 T29
C9383 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9383.2) GND_VOID=TRUE
(C9383.2) GND_VOID=TRUE
T29_A_BIAS_R2D_P1 VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF 20% 4V CERM-X5R-1 201 T29
C9381 0.47UF 20% 4V CERM-X5R-1 201 T29
R9382 1.5K 5% MF 1/20W 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
R9383 1.5K 5% MF 1/20W 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
T29_R2D_P<1> T29_R2D_N<1>
T29_A_BIAS_R2D_N1 VOLTAGE=3.3V

T29 Path Biasing

C9364 0.22UF 20% 6.3V X5R 0201 DP_SDRVA_ML_R_P<0> DP_SDRVA_ML_P<0>
C9365 0.22UF 20% 6.3V X5R 0201 DP_SDRVA_ML_R_N<0> DP_SDRVA_ML_N<0>
C9360 0.22UF 20% 6.3V X5R 0201 DP_SDRVA_ML_R_P<2> DP_SDRVA_ML_P<2>
C9361 0.22UF 20% 6.3V X5R 0201 DP_SDRVA_ML_R_N<2> DP_SDRVA_ML_N<2>

T29_D2R_C_P<0> T29_D2R_C_N<0>
D9364 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7 T29: TX_0
D9373 BAR90-02LRH TSLP-2-7 T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
D9365 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9375 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
T29_D2R_C_P<1> T29_D2R_C_N<1>

D9360 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7 T29: TX_1
D9383 BAR90-02LRH TSLP-2-7 T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
D9361 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9385 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP Path Biasing

R9361 1.5K 5% MF 1/20W 201 DP_A_BIAS_N_2 VOLTAGE=3.3V R9362 51 5% 1/20W MF 201
R9360 1.5K 5% MF 1/20W 201 DP_A_BIAS_P_2 VOLTAGE=3.3V R9363 51 5% 1/20W MF 201
R9365 1.5K 5% MF 1/20W 201 DP_A_BIAS_N_0 VOLTAGE=3.3V R9366 51 5% 1/20W MF 201
R9364 1.5K 5% MF 1/20W 201 DP_A_BIAS_P_0 VOLTAGE=3.3V R9367 51 5% 1/20W MF 201
Both R's:
C9358 0.1UF 10% 16V X5R-CERM 0201

DP A Super-Driver

=PP3V3_S0_DPSDRVA
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 20% 10V CERM 402
C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1 IN_D0P	OUT_D0P 30	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2 IN_D0N	OUT_D0N 29	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4 IN_D1P	OUT_D1P 28	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5 IN_D1N	OUT_D1N 27	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7 IN_D2P	OUT_D2P 25	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8 IN_D2N	OUT_D2N 24	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9 IN_D3P	OUT_D3P 23	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10 IN_D3N	OUT_D3N 22	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14 IN_SCL	AC_AUXP 20	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13 IN_SDA	AC_AUXN 19	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16 IN_AUXP	OUT_AUXP_SCL 18	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15 IN_AUXN	OUT_AUXN_SDA 17	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3 IN_HPD	(IPD) OUT_HPD 31	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26 I2C_CTL_EN (IPU)	CA_DET 32	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36 I2C_ADDR0 (IPD)	CEXT 11	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35 I2C_ADDR1 (IPD)		
=I2C_DPSDRVA_SCL	38 SCL_CTL		
=I2C_DPSDRVA_SDA	37 SDA_CTL		
DPSDRVA_REXT	12 REXT		
DP_AUXCH_ISOL	39 AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	34 PD (IPD)		
	GND 6	THMPAD 41	

C9319 2.2UF 20% 6.3V CERM 402-LF PLACE_NEAR=U9310.11:2 mm

SDRV_PD R9318 0 5% 1/16W MF-LF 402
R9319 4.02K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

R9370 390 5% 1/20W MF 201
R9371 390 5% 1/20W MF 201
R9352 390 5% 1/20W MF 201
R9353 390 5% 1/20W MF 201

R9354 22 5% 1/20W MF 201 DP_SDRVA_ML_R_P<0>
R9355 22 5% 1/20W MF 201 DP_SDRVA_ML_R_N<0>
R9350 22 5% 1/20W MF 201 DP_SDRVA_ML_R_P<2>
R9351 22 5% 1/20W MF 201 DP_SDRVA_ML_R_N<2>

C9363 0.1UF 10% 16V X5R-CERM 0201
C9362 0.1UF 10% 16V X5R-CERM 0201
C9367 0.1UF 10% 16V X5R-CERM 0201
C9366 0.1UF 10% 16V X5R-CERM 0201
C9369 0.1UF 10% 16V X5R 402
C9368 0.1UF 10% 16V X5R 402

AUXCH Snoop Port, used by PS8301 during training.

=PP3V3_S0_DPSDRVA
C9359 0.1UF 10% 16V X5R 402
CRITICAL U9359 74LVC1G04DBVCK SC70
DP_A_PWRDWN DP_A_BIAS
IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9390 0.1UF 10% 16V X5R-CERM 0201
C9391 0.1UF 10% 16V X5R-CERM 0201
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081 HVQFN OMIT CRITICAL

DP_SDRVA_ML_N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27 DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	26 DIN1_1-		
DP_SDRVA_AUXCH_P	19 AUX1+	DOUT_1+ 4	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_N	18 AUX1-	DOUT_1- 5	T29DPA_ML_P<1>
DP_SDRVA_HPD	17 HPD_1		T29: LSX_A_R2P/P2R (P/N)
CKPLUS_WAIVE=NdifPr_badTerm		AUX+ 6	DP_A_EXT_AUXCH_P
T29_A_RSVD_N	25 DIN2_0+	AUX- 7	DP_A_EXT_AUXCH_N
T29_A_RSVD_P	24 DIN2_0-		T29: RX_1 Bias Sink
(T29_A_LSX_P2R)	23 DIN2_1+	HPD_IN 8	DP_A_EXT_HPD
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+		
T29_D2R1_BIASN	14 AUX2-		
NC	13 HPD_2		
DP_A_PWRDWN	10 GPU_SEL		
T29_A_BIAS	32 AUX_SEL		LO=Port A HI=Port B
	11 NC		
	THMPAD GND 33 28 21		

R9392 51 5% 1/16W MF-LF 402
R9393 51 5% 1/16W MF-LF 402
R9396 1K 5% 1/16W MF-LF 402
R9397 1K 5% 1/16W MF-LF 402

SIGNAL_MODEL=T29DP_MUX

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9330 0.1UF 20% 16V CERM 402
C9331 0.1UF 20% 16V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL

DP_A_CA_DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA_CONFIG1_RC
T29_LSEO<0>	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA_CONFIG2_RC
	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	T29_A_HV_EN_R
=I2C_T29AMCU_SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29_A_UC_ADDR
=I2C_T29AMCU_SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP_A_EXT_HPD
T29DPA_HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29_A_LSX_P2R (P2R = PLUG TO RECEPTACLE)
T29_A_BIAS	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29_A_LSX_R2P (R2P = RECEPTACLE TO PLUG)
T29_LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29_LSEO<1>
T29_LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3	THRM PAD 25	

I2C Addr: 0x26/0x27 (Wr/Rd)

R9338 10K 5% 1/16W MF-LF 402
R9334 10K 5% 1/16W MF-LF 402
R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402
R9339 1M 5% 1/16W MF-LF 402

NO_T29 R9378 T29_A_BIAS 0 5% MF 1/20W 201
NO_T29 R9380 T29DPA_CONFIG1_RC 0 5% MF 1/20W 201 DP_A_CA_DET
NO_T29 R9379 T29DPA_HPD 0 5% MF 1/20W 201 DP_A_EXT_HPD
NO_T29 R9381 DP_A_PWRDWN 0 5% MF 1/20W 201

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L R9330 0 5% 1/16W MF-LF 402 SWCLK SWDIO T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC_MASTER=K62 SYNC_DATE=11/14/2016
PAGE TITLE: DisplayPort/T29 A MUXing
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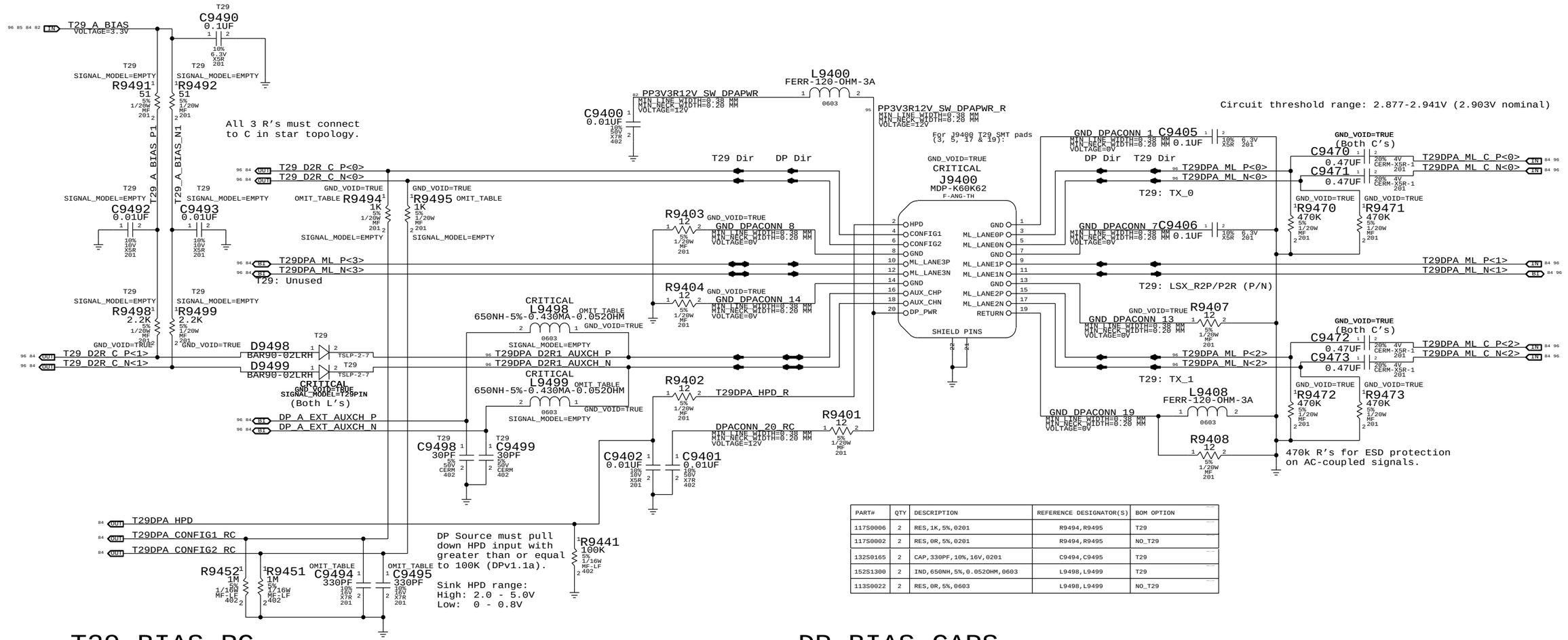
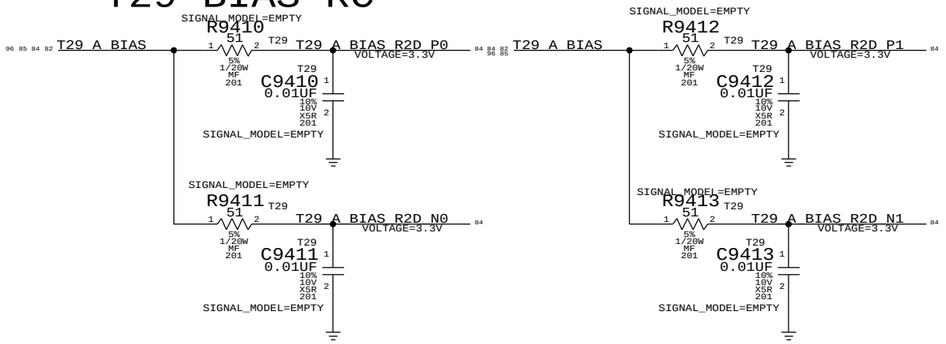
DisplayPort/T29 A Connector

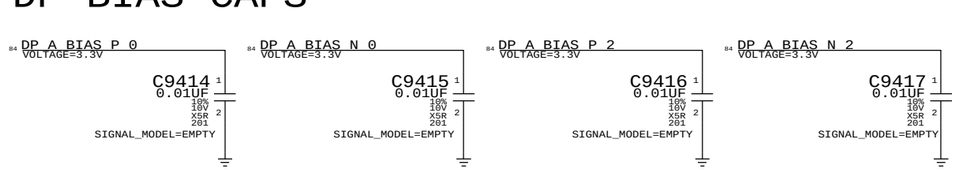


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

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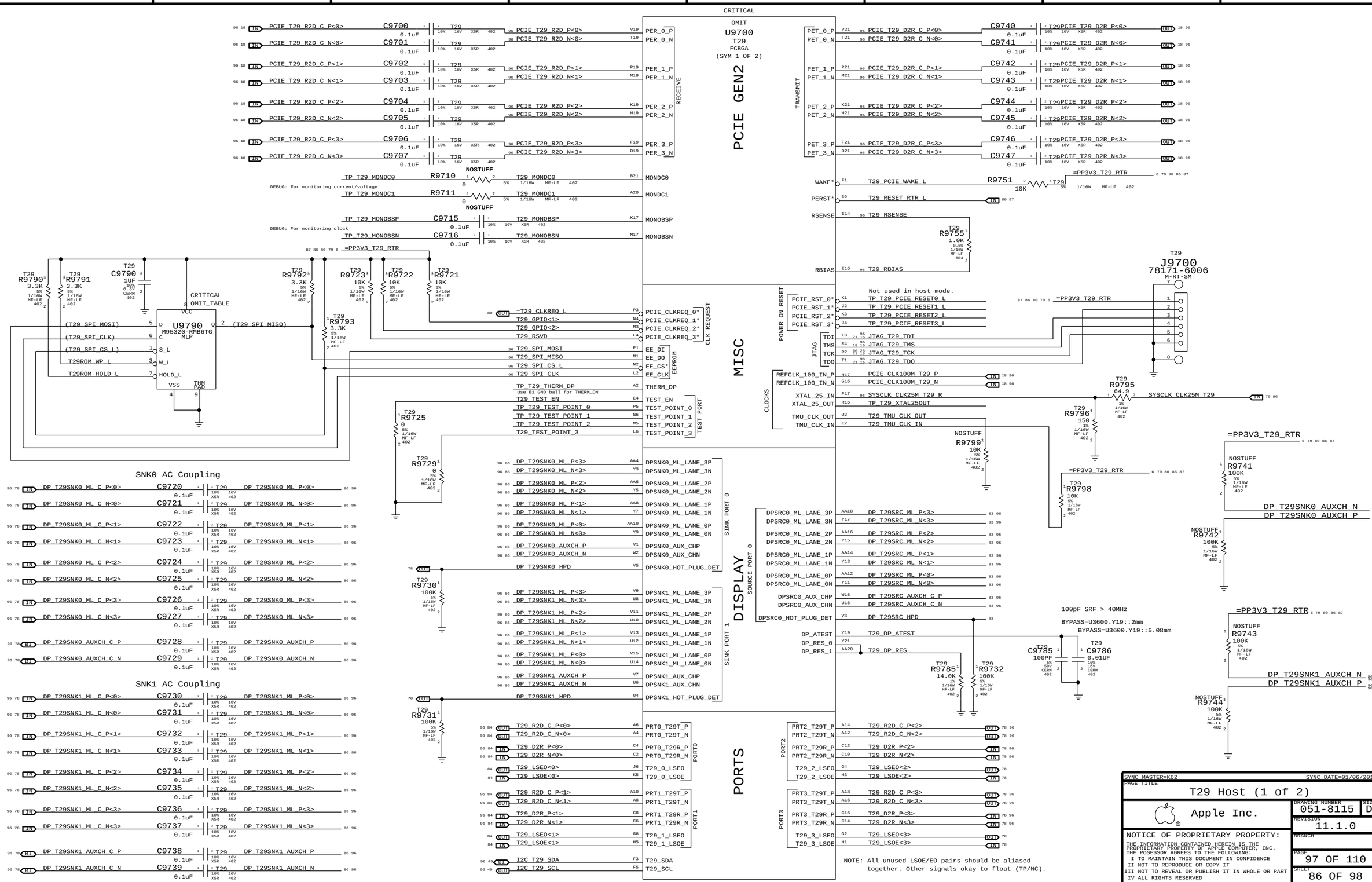

SYNC_MASTER=K62 SYNC_DATE=01/06/2013

PAGE TITLE

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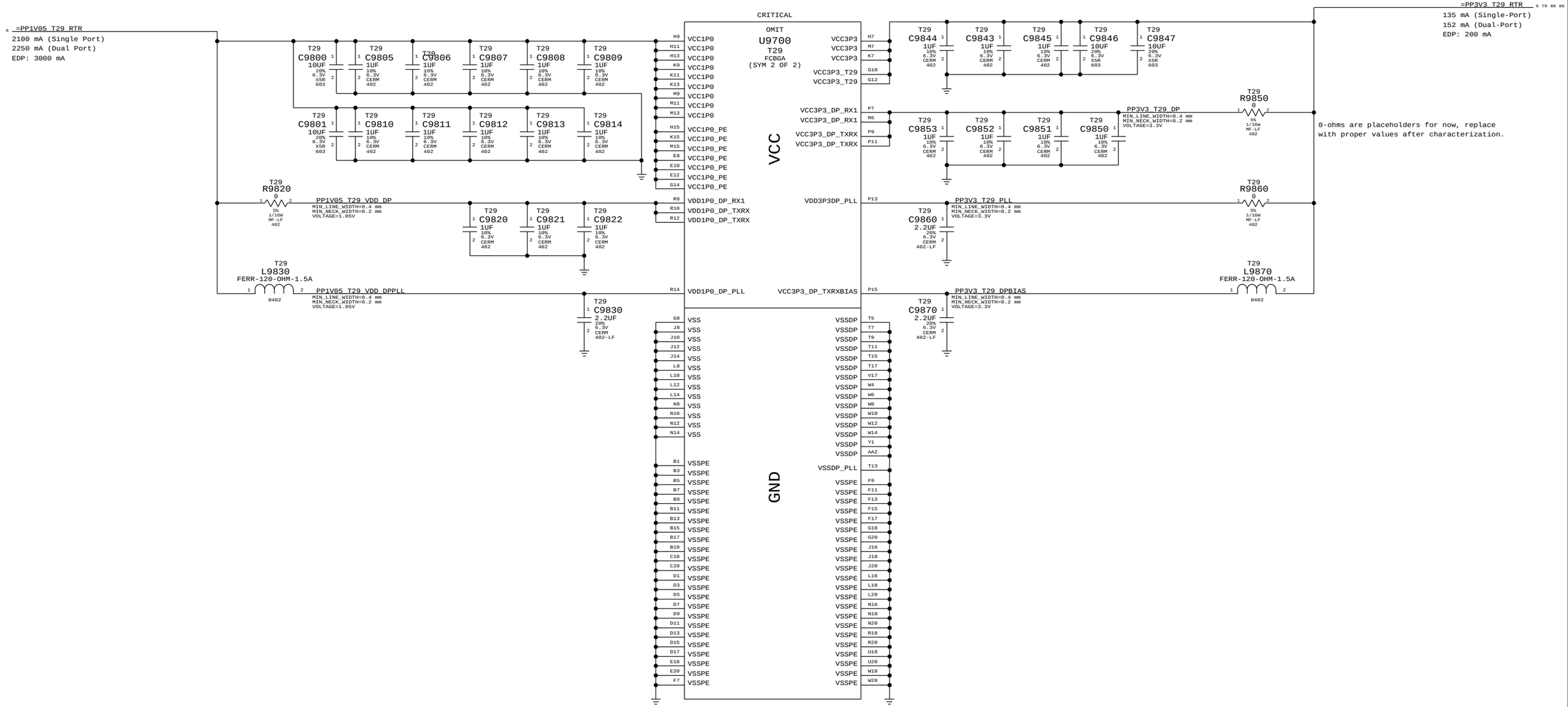

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: T29 Host (2 of 2)

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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.090 MM	=STANDARD		
34_OHM_SE	*	Y	0.19 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.090 MM	=STANDARD		
39_OHM_SE	*	Y	0.159 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.090 MM	=STANDARD		
42_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68_OHM_DIFF	ISL3,ISL6	Y	0.16 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.2 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.081 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
3.5:1_SPACING	*	0.35 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.155 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.145 MM	?
3X_DIELECTRIC	*	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.215 MM	?
4X_DIELECTRIC	*	0.305 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.285 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.355 MM	?
7X_DIELECTRIC	*	0.532 MM	?
7X_DIELECTRIC	TOP,BOTTOM	0.497 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P1P5MM	*	0.15 MM	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P1P5MM
CLK_PCIE	*	BGA	BGA_P1MM
CLK_LPC	*	BGA	BGA_P1MM
CLK_PCI	*	BGA	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CONTROL	*	*	SWITCHNODE
VR_CONTROL	VR_CONTROL	*	STANDARD
VR_CONTROL	SWITCHNODE	*	STANDARD
VR_CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: K60/K62 RULE DEFINITIONS

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
MEM_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
MEM_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2.5:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=2:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_SAMEBYTE	*	=3:1_SPACING	?
MEM_DQ_DIFFBYTE	*	=5:1_SPACING	?
MEM_DATA2MEM	*	=4:1_SPACING	?
MEM_DQS2MEM	*	=4:1_SPACING	?
MEM_2OTHER	*	=5:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE0	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE1	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE2	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE3	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE4	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE5	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE6	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE7	*	MEM_DQS2MEM
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE5	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_DQ_BYTE5	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE6	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_DQ_BYTE6	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE6	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE6	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE7	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_DQ_BYTE7	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE0	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_DQ_BYTE0	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE1	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE1	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_DQ_BYTE1	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE2	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_DQ_BYTE2	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE3	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_DQ_BYTE3	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE4	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_DQ_BYTE4	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	*	*	MEM_2OTHER

Memory Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_68D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_42S	MEM_DQ_BYTE0	MEM_A_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_A_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_A_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_A_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_A_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_A_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_A_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_A_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<7>	12 32
H17A	MEM_50S	PM	MEM_RESET_L	30 31 32 97

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_68D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_42S	MEM_DQ_BYTE0	MEM_B_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_B_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_B_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_B_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_B_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_B_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_B_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_B_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

NET_TYPE

VOLTAGE	PHYSICAL	SPACING	VOLTAGE		
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A	
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B	
H16C	MEM_POWER_PHY	MEM_POWER		CPU_DDR_VREF	11 28
H16D	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DACOUT	28
H16E	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_OPFB	28
H17C	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DQ	28
H17A	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A_SW	
H17J	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DACOUT	28
H17K	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_OPFB	28
H17P	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DQ	28
H17N	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4:1_SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=6:1_SPACING	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SATA				
H50	SATA_90D	SATA	SATA_SSD_R2D_C_P	18 42
P50	SATA_90D	SATA	SATA_SSD_R2D_C_N	18 42
N51	SATA_90D	SATA	SATA_SSD_R2D_P	42
H52	SATA_90D	SATA	SATA_SSD_R2D_N	42
K53	SATA_90D	SATA	SATA_SSD_D2R_P	18 42
K54	SATA_90D	SATA	SATA_SSD_D2R_N	18 42
K55	SATA_90D	SATA	SATA_SSD_D2R_C_P	42
K56	SATA_90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
B31	PCIE_85D	PCIE	PCIE_USB3_1_R2D_P	
A32	PCIE_85D	PCIE	PCIE_USB3_1_R2D_N	
F32	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_P	
H32	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_N	
K32	PCIE_85D	PCIE	PCIE_USB3_1_D2R_P	
J32	PCIE_85D	PCIE	PCIE_USB3_1_D2R_N	
L32	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_P	
M32	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_N	
M30	PCIE_85D	PCIE	PCIE_USB3_2_R2D_P	
M29	PCIE_85D	PCIE	PCIE_USB3_2_R2D_N	
L30	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_P	
L29	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_N	
K30	PCIE_85D	PCIE	PCIE_USB3_2_D2R_P	
K31	PCIE_85D	PCIE	PCIE_USB3_2_D2R_N	
F33	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_P	
H33	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
AM1	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
AL1	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
AH4	CPU_50S	CPU_ITP	XDP_OBSDATA_B<3..0>	25
AH3	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	25
AH1	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 25
AH2	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 25
AH4	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 25
AH5	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 25
AH6	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<7..0>	75 77
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
AL15	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	
AL16	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	
B16	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
B17	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_HDD_R2D_P	42
	SATA_90D	SATA	SATA_HDD_R2D_N	42
	SATA_90D	SATA	SATA_HDD_D2R_P	18 42
	SATA_90D	SATA	SATA_HDD_D2R_N	18 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_ODD_R2D_P	42
	SATA_90D	SATA	SATA_ODD_R2D_N	42
	SATA_90D	SATA	SATA_ODD_D2R_P	18 42
	SATA_90D	SATA	SATA_ODD_D2R_N	18 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 18
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 18
L37	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	25
L38	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
L35	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_N	26
L36	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
L39	PCIE_85D	PCIE	MXM_PCIE_R2D_P<8..15>	75 77
L40	PCIE_85D	PCIE	MXM_PCIE_R2D_N<8..15>	75 77
L42	PCIE_85D	PCIE	MXM_PCIE_D2R_P<8..15>	75 77
L43	PCIE_85D	PCIE	MXM_PCIE_D2R_N<8..15>	75 77

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PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

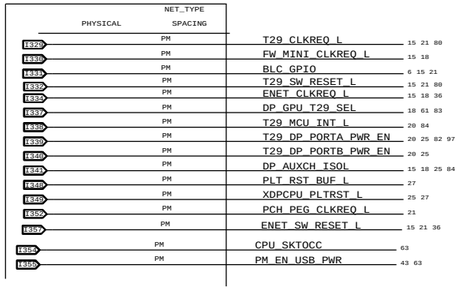
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

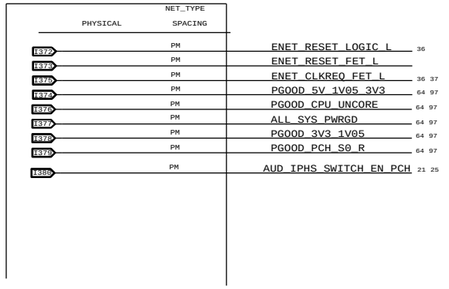
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

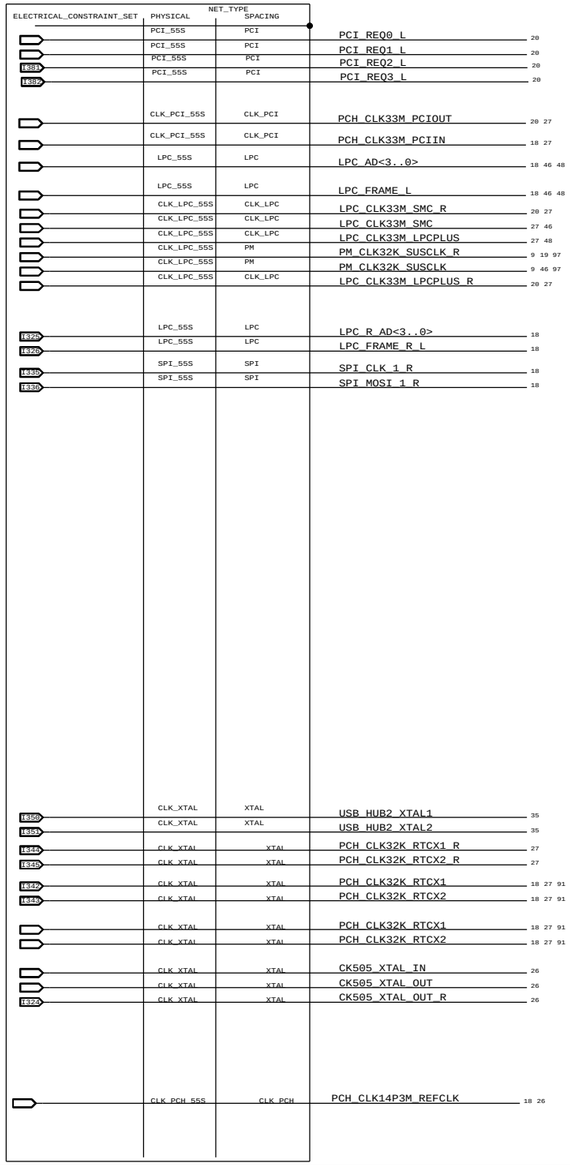
XTAL Constraints

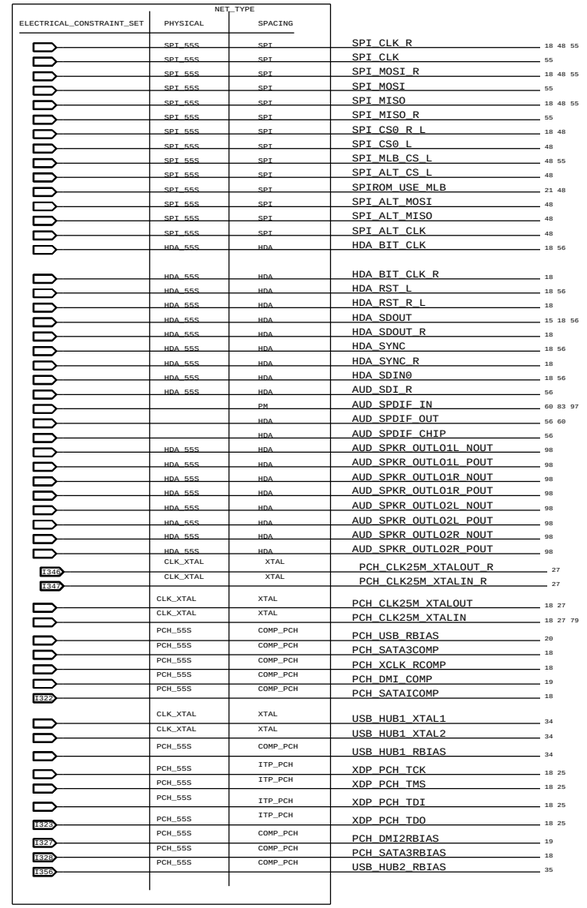
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?









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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_2OTHER	*	=50MIL_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL_SPACING	*	1.27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_DIFF_T	*	*	ENET_2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	ENET_50S	ENET_SE	ENET_RDAC 37
	CLK_PCH_5SS	XTAL	ENET_CLK25M_XTALI 36 37
	CLK_PCH_5SS	XTAL	ENET_CLK25M_XTALO 36 37
	CLK_PCH_5SS	XTAL	ENET_CLK25M_XTALO_R 36
	ENET_100D	ENET_DIFF	ENETCONN_MDI_P<3..0> 37 38
	ENET_100D	ENET_DIFF	ENETCONN_MDI_N<3..0> 37 38
	ENET_100D	ENET_DIFF_T	ENETCONN_MDI_T_P<3..0> 38
	ENET_100D	ENET_DIFF_T	ENETCONN_MDI_T_N<3..0> 38
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_P 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_N 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_P 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_N 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_C_P 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_C_N 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_C_P 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_C_N 37
	SD_50S	SD	ENET_SD_CMD 37
	SD_50S	SD	SDCONN_CMD 37 45
	SD_50S	SD	SDCONN_CLK 37 45
	SD_50S	SD	ENET_SD_CLK 37
	SD_50S	SD	SDCONN_DATA<7..0> 37 45
	SD_50S	SD	ENET_CR_DATA<7..0> 37
	SD_50S	PM	ENET_MEDIA_SENSE 15 18 37
	SD_50S	SD	ENET_MEDIA_SENSE_R
	SD_50S	SD	ENET_SD_DETECT_L 37
	SD_50S	PM	SDCONN_DETECT_BUF_L 97

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	USB_90D	USB	USB_EXTA_P 34 43
	USB_90D	USB	USB_EXTA_N 34 43
	USB_90D	USB	USB_PORT0_P 43
	USB_90D	USB	USB_PORT0_N 43
	USB_90D	USB	USB_EXTB_P 35 43
	USB_90D	USB	USB_EXTB_N 35 43
	USB_90D	USB	USB_PORT1_P 43
	USB_90D	USB	USB_PORT1_N 43
	USB_90D	USB	USB_EXTC_P 34 43
	USB_90D	USB	USB_EXTC_N 34 43
	USB_90D	USB	USB_PORT2_P 43
	USB_90D	USB	USB_PORT2_N 43
	USB_90D	USB	USB_EXTD_P 35 43
	USB_90D	USB	USB_EXTD_N 35 43
	USB_90D	USB	USB_D_MUXED_P 43
	USB_90D	USB	USB_D_MUXED_N 43
	USB_90D	USB	USB_PORT3_P 43
	USB_90D	USB	USB_PORT3_N 43
	USB_90D	USB	USB_CAMERA_P 20 44
	USB_90D	USB	USB_CAMERA_N 20 44
	USB_90D	USB	USB_CAMERA_L_P 44 98
	USB_90D	USB	USB_CAMERA_L_N 44 98
	USB_90D	USB	USB_BT_P 35 44
	USB_90D	USB	USB_BT_N 35 44
	USB_90D	USB	USB_BT_L_P 44 98
	USB_90D	USB	USB_BT_L_N 44 98
	USB_90D	USB	USB_IR_P 34 44
	USB_90D	USB	USB_IR_N 34 44
	USB_90D	USB	USB_IR_L_P 44 98
	USB_90D	USB	USB_IR_L_N 44 98
	USB_90D	USB	USB_SDCARD_P 34 44
	USB_90D	USB	USB_SDCARD_N 34 44
	USB_90D	USB	USB_SDCARD_L_P 44
	USB_90D	USB	USB_SDCARD_L_N 44
	USB_90D	USB	USB_HUB1_UP_P 20 34
	USB_90D	USB	USB_HUB1_UP_N 20 34
	USB_90D	USB	USB_HUB2_UP_P 20 35
	USB_90D	USB	USB_HUB2_UP_N 20 35
	USB_90D	USB	USB_HUB2UNUSED_P 35
	USB_90D	USB	USB_HUB2UNUSED_N 35

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
P25	CLK_PCH_5SS	XTAL	FW_CLK24P576M_XO 39
P24	CLK_PCH_5SS	XTAL	FW_CLK24P576M_XO_R 39
P26	CLK_PCH_5SS	XTAL	FW_CLK24P576M_XI 39
	FW_110D	FW_TP	FW_PORT0_TPA_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N 40 41
UNUSED FW NETS PHYSICAL PROPERTIES			
P23	FW_110D	FW_TP	FW_P1_TPA_P 39 40
P25	FW_110D	FW_TP	FW_P1_TPA_N 39 40
P24	FW_110D	FW_TP	FW_P2_TPA_P 39 40
P26	FW_110D	FW_TP	FW_P2_TPA_N 39 40
	FW_110D	FW_TP	FW_P1_TPB_P 39 40
	FW_110D	FW_TP	FW_P1_TPB_N 39 40
	FW_110D	FW_TP	FW_P2_TPB_P 39 40
	FW_110D	FW_TP	FW_P2_TPB_N 39 40

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PAGE TITLE
USB/ENET/SD/FW/AUD CONSTRAINTS

Apple Inc.

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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
ASSINGED IN CONT. MGR.

NET_TYPE	PHYSICAL	SPACING		
I16D	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0>	83
I17D	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0>	83
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P	83
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N	83
I15J	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	81 83
I15J	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	81 83
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	81 83
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	81 83
I18D	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	84
I18D	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	84
I18D	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	84
I18D	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	84
I17J	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
I17J	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
I17J	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	78 84
I17J	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	78 84
I19J	DP_85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_P	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_N	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P	
I19J	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N	
P19D	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	75 78
P20D	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	75 78
P20J	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P	75 78
P20J	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N	75 78
P20D	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	75 83
P20D	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	75 83
P20D	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P	75 83
P20D	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N	75 83
P21J	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_P	83
P21J	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_N	83
P20J	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	75 78
P20D	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	75 78
P20J	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P	75 78
P21J	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N	75 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	76 78
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	76 78

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: GRAPHICS CONSTRAINTS

Apple Inc.

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_PCH_CLK	18 49
	SMB_55S	SMB	SMBUS_PCH_DATA	18 49
	SMB_55S	SMB	SML_PCH_0_CLK	18 49
	SMB_55S	SMB	SML_PCH_0_DATA	18 49
	SMB_55S	SMB	SML_PCH_1_CLK	18 49
	SMB_55S	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_55S	SMB	SMB_BLC_TCON_SCL	6 49 81
I264	SMB_55S	SMB	SMB_BLC_TCON_SDA	6 49 81
I268	SMB_55S	SMB	I2C_TCON_SCL	81
I269	SMB_55S	SMB	I2C_TCON_SDA	81
I266	SMB_55S	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_55S	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I209	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I206	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I211	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I212	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I213	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I214	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I215	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I216	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I217	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I218	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I224	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I225	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I210	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 98
	THERM_DIFF	THERMAL	SNS_ODD_N	52 98
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 98
I223	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 98
	THERM_DIFF	THERMAL	SNS_AMB_P	52 54 98
	THERM_DIFF	THERMAL	SNS_AMB_N	52 54 98
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 98
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 95
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	95
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	95
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I253	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I252	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I241		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I240		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I242		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I238		THERMAL	SMC_DIMM_ISENSE	46 50
I228		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I226		THERMAL	SMC_VCCSA_ISENSE	46 50
I225		THERMAL	SMC_VCCSA_ISENSE_R	50
I227		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 94
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I233		THERMAL	SMC_1V05_ISENSE	46 50
I232		THERMAL	SMC_VAXG_ISENSE	46 50
I234		THERMAL	SMC_1V05_VSENSE	46 50
I235		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I237		THERMAL	SMC_VCORE_VSENSE	46 50
I239		THERMAL	SMC_CPU_VSENSE	

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PAGE TITLE: SMC Constraints

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

	PHYSICAL	SPACING	VOLTAGE	
U42	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1 66
U43	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2 66
U44	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3 66
U45	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4
U27	POWER	SWITCHNODE	1.5V	VR_AXG_PHASE1 67
U37	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE 70
U33	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE 70
U34	POWER	SWITCHNODE	1.05V	P1V05S0_PHASE 68
U42	POWER	SWITCHNODE	1.05V	P1V05_REG_PHASE
U43	POWER	SWITCHNODE	3.4V	P3V42G3H_SW 72
U44	POWER	SWITCHNODE	3.3V	ENET_3V3_S3_SR_IN 37
U37	POWER	SWITCHNODE	1.2V	ENET_SR_LX 36 37
U33	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE 71
U34	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE 71
F19	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_A 28 30
H42	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_B 28 31
H44	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_A 28 30
F64	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_B 28 31
F34	POWER	POWER	12V	PP12V_S0 6
E45	POWER	POWER	12V	PP12V_S0_CPU_FLTRD 65 66 67
E47	POWER	POWER	12V	PP12V_S0_FAN0_L 53 98
E17	POWER	POWER	12V	PP12V_S0_FAN1_L 53 98
E17	POWER	POWER	12V	PP12V_S0_FAN2_L 54 98
H27	POWER	POWER	12V	VR_CPU_DRV1_PVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV1_UVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV2_PVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV2_UVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV3_PVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV3_UVCC 66
H27	POWER	POWER	12V	VR_CPU_DRV4_PVCC
H27	POWER	POWER	12V	VR_CPU_DRV4_UVCC
H27	POWER	POWER	12V	VR_AXG_DRV1_PVCC 67
H27	POWER	POWER	12V	VR_AXG_DRV1_UVCC
H59	POWER	POWER	12V	VR_CPU_DRV1_VCC 66
H60	POWER	POWER	12V	VR_CPU_DRV2_VCC 66
H60	POWER	POWER	12V	VR_CPU_DRV3_VCC 66
H60	POWER	POWER	12V	VR_CPU_DRV4_VCC
H65	POWER	POWER	12V	PP12V_S0_VG_OK 41
H65	POWER	POWER	12V	P12V_FW_R 41
H65	POWER	POWER	12V	P12V_FW_CL 41
H65	POWER	POWER	12V	P12V_FW_D 41
H26	POWER	POWER	12V	FW_PORT0_VP 41
H27	POWER	POWER	12V	FW_PORT0_VP_F 41
H45	POWER	POWER	12V	PPVP_FW_PHY_CPS 39 41
H68	POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN 68
H76	POWER	POWER	12V	VCCSA_PWR_RC 69
H77	POWER	POWER	12V	PP12V_S0_BL_R
H77	POWER	POWER	12V	PP12V_S5_FET 6 74
H78	POWER	POWER	12V	PP12V_LCD 81
H62	POWER	POWER	12V	PP12V_G3H 6
H77	POWER	POWER	12V	PP12V_S5 6
H77	POWER	POWER	12V	PP12V_S5_RSN 74
H26	POWER	POWER	0.75V	PPVTT_S0_DDR 6
H61	POWER	POWER	0.75V	PP0V75_S0 6
H70	POWER	POWER	0.925V	PPVCCSA_S0_CPU 6
H55	POWER	POWER	1.0V	PP1V0_FW_FWPHY_AVDD 39
H57	POWER	POWER	1.0V	PP1V0_S0_FW_VDD 40
B25	POWER	POWER	1.05V	PP1V05_S0_T29 6
H76	POWER	POWER	1.05V	PPVAXG_S0 6
H77	POWER	POWER	1.05V	PP1V05_S0 6
H77	POWER	POWER	1.05V	PP1V05_S0_PCH 6
H74	POWER	POWER	1.05V	PP1V05_S0_CK505_F 26
H77	POWER	POWER	1.05V	PPVOUT_S5_PCH_DCPSUS 22
F18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F 17 22
H18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F 17 22
H18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP_F 22 24
F23	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLLDMI2_F 22 24
F18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA_F 22 24
H25	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCCLKDMI_F 22 24
H76	POWER	POWER	1.1V	PPVCORE_S0_AXG_REG1 67
H75	POWER	POWER	1.1V	PPVCORE_S0_AXG_REGOUT 67
L25	POWER	POWER	1.1V	PPVCORE_S0_CPU 6
F25	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1 66
F25	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2 66
H45	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3 66
H78	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4
H59	VR_CTL_PHY	VR_CTL	1.2V	PP1V2_S3_ENET_INTREG 36
H60	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_AVDDL 37
H65	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_PCIEPLL 37
H65	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_GPHYPLL 37
H19	POWER	POWER	1.5V	PP1V5_S0 6
H19	POWER	POWER	1.5V	PP1V5_S0_CK505_F 26
H68	POWER	POWER	1.5V	PP1V5_S0_CK505_R 26
H77	POWER	POWER	1.5V	PP1V5_S0_CPU_MEM 6
H76	POWER	POWER	1.5V	PP1V5_S0_CPU_SNS
B21	POWER	POWER	1.5V	PP1V5_S3 6
H74	POWER	POWER	1.5V	PP1V5_S3_MEM 6

POWER NET PROPERTIES

	PHYSICAL	SPACING	VOLTAGE	
U45	POWER	POWER	12V	PP12V_S0_MXM 6
H29	POWER	POWER	12V	PP12V_SLG1
H89	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1
H89	POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1
F73	POWER	POWER	1.8V	USB_HUB2_VDD1V8 35
F75	POWER	POWER	1.8V	USB_HUB2_VDD1V8PLL 35
F43	POWER	POWER	1.8V	PP1V8_S0 6
F44	POWER	POWER	1.8V	PP1V8R1V5_S0_PCH_VCCVRM_F 22 24
F56	POWER	POWER	1.8V	USB_HUB1_VDD1V8 34
F55	POWER	POWER	1.8V	USB_HUB1_VDD1V8PLL 34
H24	POWER	POWER	1.8V	PP3V3R1V8_ENET_LR_OUT_REG 37
F79	POWER	POWER	3.3V	PPVBAT_G3_SYSCLK_R 79
F68	POWER	POWER	3.3V	USB_HUB1_VDDPLL3V3 34
F66	POWER	POWER	3.3V	USB_HUB1_VDDA3V3 34
F70	POWER	POWER	3.3V	USB_HUB2_VDDPLL3V3 35
F69	POWER	POWER	3.3V	USB_HUB2_VDDA3V3 35
F21	POWER	POWER	3.3V	PP3V3R1V5_PCH_VCCSUSHDA 22 24
F21	POWER	POWER	3.3V	PP3V3_S0_CK505_F 26
F21	POWER	POWER	3.3V	PP3V3_S0_HS_F 62
F22	POWER	POWER	3.3V	PP3V3_S0_SW_SD_PWR 45
L65	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F 17 22
F22	POWER	POWER	3.3V	PP3V3_S0 6
L83	POWER	POWER	3.3V	PP3V3_SMCUSBMUX 43
F21	POWER	POWER	3.3V	PP3V3_S3 6 98
F22	POWER	POWER	3.3V	PP3V3_S3_BT_FLT 44
F66	POWER	POWER	3.3V	PP3V3_S3_MINI_CONN 33
F57	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT 44
F48	POWER	SWITCHNODE	3.3V	PP3V3_S3_ENET_PHY_FET 36
F65	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_XTALVDDH 37
F66	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_BIASVDDH 37
F66	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_AVDDH 37
F43	POWER	POWER	3.3V	ENET_XTALVDDH 37
F35	POWER	POWER	3.3V	PP3V3_S5 6
H45	POWER	POWER	3.3V	PP3V3_S5_REG_R 70
H27	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST 22
H26	POWER	POWER	3.3V	PPVOUT_PCH_DCPSUSBYP 22
H26	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC 22
H27	POWER	POWER	3.3V	PPVBATT_G3_RTC 27
H26	POWER	POWER	3.3V	PPVBATT_G3_RTC_R 27
H20	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK 60 98
H20	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VDDA 39
H20	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VP25 39
H37	POWER	POWER	3.3V	PP3V3_S0_T29 6
H10	POWER	POWER	3.3V	PP3V3_SW_DPAPWR 78 84
H82	POWER	POWER	3.3V	PP3V3_SW_DPBPWR
H82	POWER	POWER	3.3V	PP3V3_G3H_RTC 18 19 22 27
F23	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC 46 47
H25	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC 46
H66	POWER	POWER	3.42V	PP3V42_G3H 6
H77	POWER	POWER	4.5V	4V5_REG_IN 56
H24	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG 56 61
H47	POWER	POWER	4.5V	PP5V_AUDIO_HPAMP 56
H66	POWER	POWER	5V	PP5V_LAMP_VREG 56 59
H63	POWER	POWER	5V	PP5V_RAMP_VREG 58
H28	POWER	POWER	5V	PP5V_S0 6 98
H28	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC 65
H38	POWER	POWER	5V	PP5V_S0_PCH_V5REF 24
H66	POWER	POWER	5V	PP5V_S0_SATA_FET 42
H63	POWER	POWER	5V	5V_S0_P1V05REG_VIN 68
H76	POWER	POWER	5V	5V_S0_P1V05REG_VDD 68
H24	POWER	POWER	5V	PP5V_S3 6 98
F23	POWER	POWER	5V	PP5V_S3_VREFMRGN_A 28
F25	POWER	POWER	5V	PP5V_S3_VREFMRGN_B 28
H24	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT 71
H25	POWER	POWER	5V	PP5V_S3_CAMERA_FLT 44
H25	POWER	POWER	5V	PP5V_S3_REG_R 70
H24	POWER	POWER	5V	PP5V_S3_IR_FLT 44 98
H76	POWER	POWER	5V	PP5V_S5 6
H44	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS 24
H47	POWER	POWER	5V	PP5V_USB_PORT0 43
H26	POWER	POWER	5V	PP5V_USB_PORT0_F 43
H48	POWER	POWER	5V	PP5V_USB_PORT1 43
H48	POWER	POWER	5V	PP5V_USB_PORT1_F 43
H48	POWER	POWER	5V	PP5V_USB_PORT2 43
H26	POWER	POWER	5V	PP5V_USB_PORT2_F 43
H26	POWER	POWER	5V	PP5V_USB_PORT3 43
H26	POWER	POWER	5V	PP5V_USB_PORT3_F 43
H25	POWER	POWER		DDR_REG_PGND 71
H25	POWER	POWER		DDR_REG_CSGND 71
H33	POWER	POWER	3.3V	PPVDDIO_25M_B 79
H34	POWER	POWER	1.05V	PPVDDIO_25M_A 79
H35	POWER	POWER	3.3V	PPVDDIO_25M_C 79
H35	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_R 85
H37	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_D 82
H38	POWER	POWER	1.5V	PP1V5_S0_DP_R 83

SENSING NET PROPERTIES

	PHYSICAL	SPACING	
H35	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P 65 66
H35	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N 65 66
H35	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N 65
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P 65 66
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N 65 66
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N 65
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P 65 66
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N 65 66
H36	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N 65
H38	SNS_DIFF	THERMAL	VR_CPU_ISNS4_P
H38	SNS_DIFF	THERMAL	VR_CPU_ISNS4_N
H38	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N
H68	SNS_DIFF	THERMAL	P1V05S0_ISN 68
H68	SNS_DIFF	THERMAL	P1V05S0_ISP 68
H32	SNS_DIFF	THERMAL	VR_AXG_ISNS_R_P 65
H32	SNS_DIFF	THERMAL	VR_AXG_ISNS_R_N 65
H32	SNS_DIFF	THERMAL	VR_AXG_ISNS_N 65 67
H32	SNS_DIFF	THERMAL	VR_AXG_ISNS_P 65 67
H68	SNS_DIFF	THERMAL	VR_ISNS_1V05_N 94
H68	SNS_DIFF	THERMAL	VR_ISNS_1V05_P 94
H49	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N 50 94
H49	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P 50 94
H48	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N 50 94
H48	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P 50 94
H72	SNS_DIFF		CPU_VAXG_SENSE_P 13 65
H74	SNS_DIFF		CPU_VAXG_SENSE_N 13 65
H38	SNS_DIFF		VR_AXG_VSNS_R_N 65
H48	SNS_DIFF		VR_AXG_VSNS_R_P 65
H58	SNS_DIFF		VR_AXG_VSEN 65
H59	SNS_DIFF		VR_AXG_RGND 65
H71	SNS_DIFF		VR_AXG_VSNS_XW_N 65
H45	SNS_DIFF		VR_AXG_VSNS_XW_P 65
H61	SNS_DIFF		CPU_VCC_SENSE_N 13 65
H61	SNS_DIFF		CPU_VCC_SENSE_P 13 65
H61	SNS_DIFF		VR_CPU_VSEN 65
H71	SNS_DIFF		VR_CPU_RGND 65
H72	SNS_DIFF		VR_CPU_VSNS_R_N 65
H62	SNS_DIFF		VR_CPU_VSNS_R_P 65
H63	SNS_DIFF		VR_CPU_VSNS_XW_P 65
H64	SNS_DIFF		VR_CPU_VSNS_XW_N 65
H66	SNS_DIFF		CPU_VCCIO_SENSE_P 13 68
H67	SNS_DIFF		CPU_VCCIO_SENSE_N 13 68
H35	SNS_DIFF		P1V05S0_VSEN 68
H35	SNS_DIFF		P1V05S0_RTN 68

VR CTRL NET PROPERTIES

	PHYSICAL	SPACING	
F27	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH1_SNUB 66
H31	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH2_SNUB 66
H31	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH3_SNUB 66
F28	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH4_SNUB
G69	VR_CTL_PHY	VR_CTL	VR_CPU_COMP 65
H64	VR_CTL_PHY	VR_CTL	VR_AXG_TM 65
H62	VR_CTL_PHY	VR_CTL	VR_AXG_PWM_R 65
E61	VR_CTL_PHY	VR_CTL	VR_AXG_PWM 65 67
H30	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2 65 66
G62	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1 65 66
G62	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1_R 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3 65 66
H34	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R 65
F28	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4
H30	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R 65
H34	VR_CTL_PHY	VR_CTL	VR_AXG_SW_FREQ 65
H34	VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP 65
H30	VR_CTL_PHY	VR_CTL	VR_RSET 65
H30	VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP_R 65
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT1_RC 66
H35	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT2_RC 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT3_RC 66
H69	VR_CTL_PHY	VR_CONTROL	VR_AXG_BOOT1_RC 67
H35	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT4_RC
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_BOOT 66
H30	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_LGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_UGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_BOOT 66
H30	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_LGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_UGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_BOOT 66
H30	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_LGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_UGATE 66
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_BOOT
H30	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_LGATE
H30	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_UGATE
H69	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_BOOT 67
H69	VR_CTL_PHY	VR_CTL	VR_AXG_DRV1_UGATE_R 67
H69	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_LGATE 67
H69	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_UGATE 67
H30	VR_CTL_PHY	VR_CTL	VR_CPU_SW_FREQ 65
H30	VR_CTL_PHY	VR_CTL	VR_CPU_FB 65
H30	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R 65
H30	VR_CTL_PHY	VR_CTL	VR_CPU_RAMP_ADJ
E35	VR_CTL_PHY	VR_CTL	VR_CPU_IMON 50 65
L63	VR_CTL_PHY	VR_CTL	VR_CPU_SUTH 65
L63	VR_CTL_PHY	VR_CTL	VR_CPU_N_PSI 65
H30	VR_CTL_PHY	VR_CTL	VR_CPU_FDVID 65
E43	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP 65
L63	VR_CTL_PHY	VR_CTL	VR_CPU_IAUTO 65
E64	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP1 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP2 65
E44	VR_CTL_PHY	VR_CTL	VR_CPU_FB_RC 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_FB2 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_IMON_R 65
H34	VR_CTL_PHY	VR_CTL	VR_CPU_HFREQ_COMP 65
H68	VR_CTL_PHY	SWITCHNODE	VR_AXG_PH1_SNUB 67
H62	VR_CTL_PHY	VR_CTL	VR_AXG_IMON 50 65
H65	VR_CTL_PHY	VR_CTL	VR_AXG_IMON_R 65
H62	VR_CTL_PHY	VR_CTL	VR_AXG_HFREQ_COMP 65
H33	VR_CTL_PHY	VR_CTL	VR_AXG_FB 65
H62	VR_CTL_PHY	VR_CTL	VR_SEN_R1 65
H33	VR_CTL_PHY	VR_CTL	VR_SEN_R2 65
H33	VR_CTL_PHY	VR_CTL	VR_SEN_R3 65
H30	VR_CTL_PHY	VR_CTL	VR_AXG_COMP_RC 65
H30	VR_CTL_PHY	VR_CTL	VR_AXG_COMP 65
H33	VR_CTL_PHY	VR_CTL	VR_AXG_TCOMP 65
H35	VR_CTL_PHY	SWITCHNODE	P1V05S0_UGATE 68
H30	VR_CTL_PHY	SWITCHNODE	P1V05S0_LGATE 68
H30	VR_CTL_PHY	VR_CTL	P1V05S0_BOOT 68
H68	VR_CTL_PHY	VR_CTL	P1V05S0_BOOT_R 68
F24	VR_CTL_PHY	VR_CTL	P1V05_IMON 50 68
H32	VR_CTL_PHY	VR_CTL	P1V05S0_FB 68
H30	VR_CTL_PHY	VR_CTL	P1V05S0_PHASE_L 68
H69	VR_CTL_PHY	VR_CTL	P1V05S0_VW 68
H64	VR_CTL_PHY	VR_CTL	P1V05S0_COMP 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_ICOMP 68
H40	VR_CTL_PHY	VR_CTL	P1V05_S0_VDIFF 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_COMP_C 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_VDIF_C 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_VO 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_OCSET 68
H40	VR_CTL_PHY	VR_CTL	P1V05S0_SNUBBER 68
F38	VR_CTL_PHY	VR_CTL	P1V05_REG_VFB
H26	VR_CTL_PHY	VR_CTL	ENET_SR_VFB 36 37
H76	VR_CTL_PHY	VR_CTL	P1V05S0_ISP_R 68
H80	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R 69 95
H80	VR_CTL_PHY	VR_CTL	T29BST_FBX
H67	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST 72
H68	VR_CTL_PHY	VR_CTL	P3V42G3H_FB 72

VR CTRL NET PROPERTIES

	PHYSICAL	SPACING	
H37	VR_CTL_PHY	VR_CTL	DDR_REG_CS 71
H36	VR_CTL_PHY	VR_CTL	DDR_REG_FB 71
H38	VR_CTL_PHY	VR_CONTROL	DDR_REG_LGATE 71
H36	VR_CTL_PHY	VR_CONTROL	DDR_REG_UGATE 71
H44	VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT 71
H42	VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT_R 71
H42	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS 71
H44	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS 71
H24	VR_CTL_PHY	VR_CTL	DDR_REG_PHASE_R 71
H77	VR_CTL_PHY	VR_CTL	DDR_REG_UGATE_R 71
H26	VR_CTL_PHY	SWITCHNODE	1V5_SNUBBER 71
H26	VR_CTL_PHY	VR_CTL	P1V8_REG_VFB 71
H27	VR_CTL_PHY	VR_CTL	P1V8_REG_SYNC 71
H36	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT 70
H36	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT_R 70
H36	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB 70
H34	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN 70
H35	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_LGATE 70
H34	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET 70
H34	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_VOUT1 70
H70	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_FSET1 70
H34	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_UGATE 70
H57	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB 70
H35	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_BOOT 70
H46	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB 70
H46	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN 70
H46	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_LGATE 70
H46	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET 70
H46	VR_CTL_PHY	VR_CTL	P5VS3_REG_FSET2 70
H46	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_UGATE 70
H47	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_VOUT2 70
H48	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT1 69
H48	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2 69
F55	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R 69 95
H20	VR_CTL_PHY	VR_CTL	VCCSA_OUT 69
H24	VR_CTL_PHY	VR_CTL	VCCSA_GATE 69
H30	VR_CTL_PHY	VR_CTL	VCCSA_REF 69
H31	VR_CTL_PHY	VR_CTL	VCCSA_CRL 69
H23	VR_CTL_PHY	VR_CTL	CPU_VCCSA_SENSE 13 69
H29	VR_CTL_PHY	VR_CTL	VR_CPU_TM 65
H32	VR_CTL_PHY	PM	3V3R2V9_DPAPWR_ADJ 82 97

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

	PHYSICAL	SPACING	
H75	VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK_R 13
H72	VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L_R 13
H75	VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT_R 13
L49	VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK 13 65
L49	VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L 13 65
L50	VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT 13 65

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2x_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING (NET_TYPE)	
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P 84 85
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N 84 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0> 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P 18 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N 18 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N 83 86
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING (NET_TYPE)	
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI 15 21 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS 15 18 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK 15 21 25 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO 15 21 86
U43?	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 86
U43?	T29_SPI_55S	T29_SPI	T29_SPI_MISO 86
U43?	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 86
U44?	T29_SPI_55S	T29_SPI	T29_SPI_CLK 86
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
	T29_SMB_55S	T29_SMB	I2C_T29_SDA 49 86
	T29_SMB_55S	T29_SMB	I2C_T29_SCL 49 86
U42?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 79
U42?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET 79
U42?	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC 36 79
U42?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK 79
U43?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
U42?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
U42?	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2 79
U42?	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R 79
U42?	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1 79
U43?	T29_55S	T29_COMP	T29_RSENSE 86
U43?	T29_55S	T29_COMP	T29_RBIAS 86
U43?		T29_COMP	T29_A_BIAS 82 84 85
U43?		T29_COMP	T29_B_BIAS
U42?		T29_COMP	DP_A_BIAS 84

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I357	PM	4V5_REG_EN	56
I358	PM	3V42G3H_SHDN_L	72
I359	PM	ALL_SYS_PWRGD_R	5 32 64
I360	PM	ALL_SYS_PWRGD_SMC	46 64
I361	PM	AP_PWR_EN	20 25 33
I362	PM	AP_MINI_RESET_L	93
I363	PM	AUD_I2C_INT_L	20 62
I364	PM	AUD_IP_PERIPHERAL_DET	20 61
I365	PM	AUD_IPHS_SWITCH_EN	21 62
I366	PM	AUD_SPDIF_IN	60 83 91
I367	PM	AUD_SPDIF_IN_CODEC	56 83
I368	PM	BDV_BKL_PWM	46 83 97
I369	PM	BL_PWM	6 83
I410	PM	BL_EN	6 81
I411	PM	BDV_BKL_PWM	46 83 97
I369	PM	CK505_27MHZ_EN	26
I370	PM	CPUVTT_REG_EN	
I371	PM_VTT	CPUVTT_REG_PGOOD_R	63
I372	PM	CPU_MEM_RESET_L	11 32
I373	PM	CPU_PECI_R	46
I374	PM_VTT	CPU_PWRGD	11 21 25
I375	PM	CPU_RESET_L	11 27
I376	PM	CPU_SKTOCC_L	11 63
I377	PM	CPU_CATERR_L	11
I378	PM	CPU_PECI	11 21 46
I379	PM	CPU_PROCHOT_L	11 47 65
I380	PM	CPU_THRMTRIP_L	11 47
I381	PM	CPU_PROC_SEL	11 19
I382	PM	DEBUG_RESET_L	27 48
I383	PM	DDRVTT_EN	
I384	PM	DP_INT_SPDIF_AUDIO	81 83
I385	PM	DP_INTPNL_HPD	81 83
I386	PM	3V3R2V9_DPAPWR_ADJ	82 95
I387	PM	DP_A_PWRDWN	84
I388	PM	DP_A_PWRDWN_FET_R	82
I389	PM	DP_A_PWRDWN_INV	82
I390	PM	DPAPWRSW_HVEN_L_R	82
I391	PM	DPAPWRSW_CT	82
I392	PM	DPAPWRSW_ILIM	82
I393	PM	DPAPWRSW_IFLT	82
I394	PM	T29_A_HV_EN	82 84
I395	PM	3V3R2V9_DPBPWR_ADJ	
I396	PM	DP_B_PWRDWN	
I397	PM	DP_B_PWRDWN_FET_R	
I398	PM	DP_B_PWRDWN_INV	
I399	PM	DPBPWRSW_HVEN_L_R	
I400	PM	DPBPWRSW_CT	
I401	PM	DPBPWRSW_ILIM	
I402	PM	DPBPWRSW_IFLT	
I403	PM	T29_B_HV_EN	
I404	PM	T29_PWR_EN	18 80 97
I429	PM	T29_RESET_RTR_L	80 86
I405	PM	LCD_BL_FILT	83
I406	PM	LCD_BLK_ON_DLY	
I407	PM	LCD_BL_PWM	83
I408	PM	MXM_PNL_BL_PWM	76 83

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I230	PM	ENET_PWR_EN	20 25 36
I229	PM	ENET_LOW_PWR	15 21 37
I229	PM	FW_RESET_L	27 39
I231	PM	ENET_RESET_L	27 36
I236	PM	FW_PME_L	15 21 39
I237	PM	FW_PWR_EN	15 21
I235	PM	FW_CLKREQ_L	15 39
I248	PM	ISOLATE_CPU_MEM_L	21 25 32
I260	PM	LPC_PWRDWN_L	19 46 48
I269	PM	MEM_RESET_L	30 31 32 89
I262	PM	MINI_CLKREQ_L	15 33
I263	PM	MINI_RESET_L	27 33
I264	PM	MXM_CLKREQ_L	9 75
I267	PM	MXM_GOOD	5 21 25
I272	PM	ODD_PWR_EN_L	15 21 42
I68	PM	RTC_RESET_L	18 27 97
I48	PM	RSMRST_PWRGD	46 64
I47	PM	RTC_RESET_L	18 27 97
I331	PM	S4_ENABLES	63
I480	PM	SDCONN_STATE_RST_L	
I481	PM	SDCONN_DETECT_BUF_L	92
I482	PM	SDCONN_STATE_CHANGE	20 25 45
I483	PM	SDCARD_RESET	15 21 44 98
I434	PM	SDCARD_RESET_L	44
I435	PM	SDCARD_PLT_RST_L	27 44
I436	PM	SDCARD_PLT_RST_L_R	
I435	PM	SMC_PM_G2_EN	46 74
I432	PM	SMC_PM_G2_EN_R	74
I433	PM	SMC_PM_G2_EN_L	74
I485	PM	S5_DG_1	74
I486	PM	S5_MSFT_G1	74
I441	PM	USE_HDD_OOB_L	20 51
I442	PM	HDD_OOB_1V00_REF	51
I440	PM	SMC_ADAPTER_EN	19 46 47
I438	PM	SMC_RUNTIME_SCI_L	21 46 47
I439	PM	SMC_WAKE_SCI_L	15 18 21 46
I428	PM	SMC_DELAYED_PWRGD	47 64
I428	PM	SMC_LRESET_L	27 46
I429	PM	SMC_RESET_L	46 47 48
I431	PM	SMC_PROCHOT	46 47
I437	PM	SMC_PROCHOT_3_3_L	46 47
I444	PM	SMC_ONOFF_L	46 47
I443	PM	SMC_MANUAL_RST_L	47
I259	PM	SPI_DESCRIPTOR_OVERRIDE_L	18 46
I446	PM	T29_PWR_EN	18 80 97
I450	PM	T29_RESET_L	27 80
I448	PM	T29_DP_PORTA_PWR_EN	20 25 82 91
I449	PM	T29_DP_PORTA_PWR_EN_REG	82
I265	PM_VTT	XDP_CPUPWRGD	
I261	PM_VTT	XDP_DBRESET_L	11 25
I266	PM_VTT	XDP_PWRGD	
I268	PM	XDPPCH_PLTRST_L	25 27
I256	PM	USB_HUB_SOFT_RESET_L	20 25 34
I424	PM	VSYNC_DP_CONN	6 81
I424	PM	VSYNC_DP	81
I424	PM	VIDEO_ON	81
I844	PM	VTT_REG_PGOOD_L	63

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I272	PM	PLT_RESET_L	20 27
I442	PM_VTT	PLT_RESET_LS1V05_L	11
I274	PM	PM_BATLOW_L	15 19 46
I275	PM	PM_CLK32K_SUSCLK	9 46 91
I276	PM	PM_CLK32K_SUSCLK_R	9 19 91
I277	PM	PM_CLKRUN_L	15 19 46 48
I278	PM	PM_PWRBTN_L	19 25 46
I279	PM	PM_RSMRST_L	27 46
I280	PM	PM_RSMRST_PCH_L	19 27
I281	PM	PCH_SRTCRST_L	18
I282	PM	PCH_INTVRMEN_L	18
I141	PM	PCH_DSWVRMEN	19
I139	PM	PCH_DF_TVS	19
I152	PM	PCH_PROCPWRGD	21
I283	PM	PCIE_WAKE_L	19 33 36 78
I442	PM	PM_DSW_PWRGD	19
I443	PM	PM_ASW_PWRGD	19 64
I444	PM	PM_MEM_PWRGD_R	11
I450	PM	PM_EN_DDR1V5_S3_REG	63 71
I451	PM	PM_EN_DDRVTT_S0_REG	32 63 71
I452	PM	PM_EN_P12V_S0_FET	6 63
I453	PM	PM_EN_P1V05_S0_REG	63 68
I470	PM	PM_EN_P1V05_S3_REG	
I473	PM	PM_EN_P1V5_S0_FET	63 73
I472	PM	PM_EN_P1V8_S0_REG	63 71
I475	PM	PM_EN_P3V3_S0_FET	63 73
I476	PM	PM_EN_P3V3_S3_FET	63 73
I477	PM	PM_EN_P3V3_S5_REG	70
I478	PM	PM_EN_P5V_S0_FET	63 73
I479	PM	PM_EN_P5V_S3_REG	63 70
I480	PM	PM_EN_PVCCSA_S0_REG_L	64
I455	PM	PM_EN_VCCSA_S0_CPU	
I470	PM	PM_EN_PVCORE_CPU	63 65
I438	PM_VTT	PM_MEM_PWRGD	11 19 97
I454	PM	PM_MXM_EN	64 76
I332	PM	PM_PCH_PWRGD_R	64
I333	PM	PM_PECI_PWRGD	46 64
I335	PM	PM_PECI_PWRGD_R	46
I438	PM	PM_PGOOD_DDR1V5_S3_REG	5 63 71
I437	PM	PM_PGOOD_P1V05_S0_REG	63 64 68
I439	PM	PM_PGOOD_P1V5_S0_FET	11 64 73
I440	PM	PM_PGOOD_P1V8_S0_REG	64 71
I436	PM	PM_PGOOD_P3V3_S0_FET	63 64 73
I441	PM	PM_PGOOD_P3V3_S3_FET	34 73
I442	PM	PM_PGOOD_P3V3_S5_REG	27 64 70
I443	PM	PM_PGOOD_P5V_S0_FET	63 64 73
I444	PM	PM_PGOOD_MINI	33
I445	PM	PM_PGOOD_PVCORE_CPU	5 25 64 65
I285	PM	PM_PGOOD_PVCCSA_S0_REG	63 64
I286	PM	PM_PGOOD_P5V_S3_REG	63 70 82
I287	PM	PM_PGOOD_PVAXG	5 65
I438	PM_VTT	PM_MEM_PWRGD	11 19 97
I444	PM	PM_MEM_PWRGD_L	11
I254	PM	PM_MXM_PGOOD	64 76
I253	PM	PM_PCH_PWRGD	19 21 64
I289	PM	PM_SLP_S3_5V	32
I293	PM	PM_SLP_S3_5V_L	32
I294	PM	PM_SLP_S3_5V_R2	32
I295	PM	PM_SLP_S3_L	5 19 26 32 36 46 47 63 82
I242	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
I243	PM	PM_SLP_S5_L	5 19 46 47 63
I297	PM_VTT	PM_SYNC	11 19
I298	PM	PM_SYSRST_L	19 25 27 46
I300	PM	PM_SYS_PWRGD	19 32 64
I301	PM_VTT	PM_THRMTRIP_L	21 47
I302	PM	PM_SLP_S3_BUF_L	63
I303	PM	PM_SLP_S4_1_1_R	63
I304	PM	PM_SLP_S4_D_L	32
I305	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
I438	PM	PGOOD_P1V5_S0_DLY	11
I439	PM	PGOOD_1V8_S0_G1	64
I440	PM	PGOOD_1V8_S0_G2	64
I480	PM	PGOOD_P12V_S0	63 64
I310	PM	PGOOD_P1V8_S0	64
I311	PM	PGOOD_PCH_S0	5 64
I450	PM	PGOOD_PCH_S0_R	64 91
I315	PM	PGOOD_SYSPWROK	64
I316	PM	PGOOD_SYSPWROK_R	64
I318	PM	POWER_BUTTON_L	47
I331	PM	PEG_RESET_L	9 27
I431	PM	PGOOD_CPU_S0	64
I422	PM	PGOOD_CPU_UNCORE	64 91
I424	PM	PGOOD_5V_1V05_3V3	64 91
I420	PM	PGOOD_3V3_1V05	64 91
I426	PM	PGOOD_12V_S0_G1	64
I429	PM	PGOOD_12V_S0_G2	64
I422	PM	9V_COMP_REF	64
I426	PM	12V_COMP_REF	64
I430	PM	ALL_SYS_PWRGD	64 91

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

95 6	IN	PP5V_S3	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
92 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
92 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE
92 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
92 44	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

97 44 21 15	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

92 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
92 44	IN	USB_IR_L_N	FUNC_TEST=TRUE
95 44	IN	PP5V_S3_IR_FLT	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

94 52	IN	SNS_ODD_P	FUNC_TEST=TRUE
94 52	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

53	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH0_L	FUNC_TEST=TRUE
95 53	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
53	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

54	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
54	IN	FAN_TACH2_L	FUNC_TEST=TRUE
95 54	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
54	IN	FAN_2_GND	FUNC_TEST=TRUE
94 54 52	IN	SNS_AMB_P	FUNC_TEST=TRUE
94 54 52	IN	SNS_AMB_N	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH1_L	FUNC_TEST=TRUE
95 53	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
53	IN	FAN_1_GND	FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

94 51 42	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

94 52 44	IN	SNS_SKIN_LEFT_P	FUNC_TEST=TRUE
94 52 44	IN	SNS_SKIN_LEFT_N	FUNC_TEST=TRUE
94 52	IN	SNS_SKIN_RIGHT_P	FUNC_TEST=TRUE
94 52	IN	SNS_SKIN_RIGHT_N	FUNC_TEST=TRUE

J6602 AUDIO RIGHT SPEAKER

91	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

91	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S

95 60	IN	PP3V3_AUDIO_SPDIF_JACK	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60	IN	AUD_LI_DET_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_L_JACK	FUNC_TEST=TRUE
60	IN	HS_MIC_HI_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_L_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TYPEDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_IP_PERPH_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TIPDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_SPDIFIN_JACK	FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

		GND	17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17
95 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
95 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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